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2 General Description

The CVC in an enhanced version of CAMAC crate controller with VSB differential bus (VDB) interface. It is based on a MC-68030 20 MHz microprocessor.

The stand alone version of the CVC contains the following components:
- VDB master/slave interface
- CAMAC sequencer
- up to 15 Mbytes static RAM
- up to 4 Mbit EPROM
- two serial I/O ports
- SCSI controller
- cheapernet interface
- local extension bus (LEB) connector (communication and system upgrades)

2.1 Power Requirements

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Requirements</td>
<td>full equipped</td>
</tr>
<tr>
<td>on + 5 Volts (+ 6 V from CAMAC crate)</td>
<td>4.5 A</td>
</tr>
<tr>
<td>on +/- 12 Volts</td>
<td>100 mA</td>
</tr>
</tbody>
</table>
### 2.2 Front Panel Description

Fig. 1 Front Panel of CVC4

<table>
<thead>
<tr>
<th>Label on CVC Front-panel</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN QX (LED)</td>
<td>enabled CAMAC X and Q response with CAMAC data</td>
</tr>
<tr>
<td>HALT (LED)</td>
<td>CPU is in HALT state</td>
</tr>
<tr>
<td>VIRQ (LED)</td>
<td>active VDB slave interrupt</td>
</tr>
<tr>
<td>SDRQ (LED)</td>
<td>SCSI controller is in Direct Buffer Mode (DBA)</td>
</tr>
<tr>
<td>MASTER (LED)</td>
<td>CVC is master on the VDB</td>
</tr>
<tr>
<td>TERM. ON (LED)</td>
<td>VDB terminator board placed on CVC</td>
</tr>
<tr>
<td>BT EN (LED)</td>
<td>enabled VDB master block transfer</td>
</tr>
<tr>
<td>CPU STATUS (LED)</td>
<td>shows CPU activity</td>
</tr>
<tr>
<td>ABORT RESET (switch)</td>
<td>dual function switch: Reset CPU (&lt;&gt;) ABORT interrupt</td>
</tr>
<tr>
<td>CR# (switch)</td>
<td>crate number selection switch. crate number zero configures CVC as VDB master</td>
</tr>
<tr>
<td>TERM/HOST (connector)</td>
<td>terminal and host connector</td>
</tr>
<tr>
<td>LAN (coaxial connector)</td>
<td>cheapernet 50 Ω cable connector</td>
</tr>
<tr>
<td>HD (LED)</td>
<td>hard disk activity LED</td>
</tr>
<tr>
<td>SCSI (connector)</td>
<td>50 pin SCSI connector</td>
</tr>
<tr>
<td>VDB (connector)</td>
<td>96 pin VGA cable connector for VDB</td>
</tr>
</tbody>
</table>
### 2.3 Block Diagram

Fig. 2 Block Diagram of CVC4

**Abbreviations used in the above Block Diagram**

- **FPU**: Floating Point Unit
- **CPU**: 68030 Central Processor
- **VSB**: Differential Bus Interface
- **MEM**: up to 15 Mbytes static or dynamical RAM
- **IPIN**: Cheapernet (Ethernet) Interface
- **NAFR**: Register for CAMAC crate number, subaddress and function code
- **IRQ**: Interrupt Request Controller
- **CWR**: CAMAC Write Register
- **CRR**: CAMAC Read Register
- **LBUF**: LAM Buffer (Interrupt)
- **CSR**: Control and Status Register
- **SIO**: Serial I/O Interface
- **LRAM**: Local RAM
- **RTC**: Real Time Clock
3 CVC Addressing Overview

The internal resources of the CVC are selected with address bits 30, 27 - 26 and 20 - 16.

**Note:** All addresses in the table below are CPU addresses.

For VDB slave addresses see section 6

Table 1: Addressing Overview

<table>
<thead>
<tr>
<th>Source or Destination</th>
<th>Address (hexadecimal notation)</th>
<th>Long word (LW), Word (W) or Byte (B) Access</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>from</td>
<td>to</td>
</tr>
<tr>
<td>EPROM 1 Mbit</td>
<td>0000 0000</td>
<td>0001 FFFE</td>
</tr>
<tr>
<td>2 Mbit</td>
<td>0000 0000</td>
<td>0003 FFFE</td>
</tr>
<tr>
<td>4 Mbit (max.)</td>
<td>0000 0000</td>
<td>0007 FFFE</td>
</tr>
<tr>
<td>NVRAM (32 kB, nonvolatile)</td>
<td>000F 8000</td>
<td>000F FFFF</td>
</tr>
<tr>
<td>CRAM (CPU RAM, 15 MB max.)</td>
<td>0010 0000</td>
<td>00FF FFFF</td>
</tr>
<tr>
<td>VRAM (RAM area accessed over VDB slave interface)</td>
<td>0400 0000</td>
<td>0417 FFFC</td>
</tr>
<tr>
<td>CAMAC standard cycle (1 µs bus cycle)</td>
<td>0418 0000</td>
<td>0418 FFFC</td>
</tr>
<tr>
<td>CAMAC short cycle (600 ns bus cycle)</td>
<td>0419 0000</td>
<td>0419 FFFC</td>
</tr>
<tr>
<td>2nd CAMAC standard cycle (1 µs bus cycle)</td>
<td>041E 0000</td>
<td>041E FFFC</td>
</tr>
<tr>
<td>CRR (CAMAC read register)</td>
<td>041A 0000</td>
<td>LW</td>
</tr>
<tr>
<td>CSR (control and status register)</td>
<td>041B E6C0</td>
<td>LW</td>
</tr>
<tr>
<td>2nd CSR (control and status register)</td>
<td>041B E4C0</td>
<td>LW</td>
</tr>
<tr>
<td>CLB (CAMAC LAM buffer)</td>
<td>041C 0000</td>
<td>LW</td>
</tr>
<tr>
<td>VDB master interface</td>
<td>0800 0000</td>
<td>0BFF FFFC</td>
</tr>
<tr>
<td>Serial I/O (terminal and host interface)</td>
<td>0C00 0000</td>
<td>0C00 000F</td>
</tr>
<tr>
<td>Cheapernet IPIN (ELTEC local extension bus)</td>
<td>0C01 0000</td>
<td>0C01 000F</td>
</tr>
<tr>
<td>RTC (real time clock)</td>
<td>0C02 0000</td>
<td>0C02 000F</td>
</tr>
<tr>
<td>SCSI (or extension port)</td>
<td>0C03 0000</td>
<td>0C03 FFFF</td>
</tr>
<tr>
<td>IRQ (interrupt controller)</td>
<td>0C04 0002</td>
<td>0C04 0003</td>
</tr>
</tbody>
</table>
4 CVC Memory

4.1 EPROM
The EPROM memory is placed in 44 Pin LCC socket on the CVC board. The address space of the EPROM is \( \text{hex. 00000000 - 007FFFE} \) maximal.

Three versions of EPROMs are available: 1, 2 and 4 Mbit. If the EPROM with 1 or 2 Mbit capacity is used, the 0 ohm resistor R1 shall be soldered at the CVC printed board, if 4 Mbit version of EPROM is used, the 0 ohm resistor R2 shall be soldered instead. The data width of the CVC EPROM is 16 bit.

4.2 CRAM (CPU RAM)
The random access memory of CVC is placed on a piggyback board. Several versions of CVC memory piggyback boards exists: The 1, 2 or 3 Mbytes SRAM boards with zero wait state (100 ns CPU access), 4 Mbytes SRAM board with zero wait state 150 ns CPU access. Up to 16 Mbytes memory can be addressed on CVC the piggyback board. All versions of the memory are connected to a full 32 bit wide data bus. The full address space for CPU memory CRAM is \( \text{hex. 00100000-00FFFFFF} \). Over this address space the memory can be accessed as byte, word and long word memory.

4.3 NVRAM
NVRAM is a 32k x 8 organized static RAM with battery backup circuit. Writing into the NVRAM can be enabled with CSR bit 02 set to 1. After power up and reset, writing into NVRAM is disabled. The NVRAM can be accessed from the CPU only.

4.4 VRAM (VDB RAM)
The CVC random access memory can be accessed over two address spaces, one is the earlier mentioned CRAM address space and the other is the VDB-slave VRAM address space. Over VRAM address space only the lower 1.5 Mbytes of the CVC memory can be accessed, so that the lower 1.5 Mbytes of CRAM and VRAM is the same memory, reachable over different address spaces. The external VDB address of memory is \( \text{hex. 00000000..0017FFFC} \), this address is converted at the VDB interface to the internal address of \( \text{hex. 04000000..0417FFFC} \) and corresponds to \( \text{hex. 00100000..0027FFFF} \) of CRAM.

Next page: Fig. 3: Address Space Overview
Fig. 3: Address Space Overview

- **VDB master**
  - LBUF
  - CSR
  - CAMAC

- **CVC slave**
  - IRQ Controller
  - SCSI/PORT
  - RTC
  - Cheapernet
  - Serial I/O

Hexadecimal addresses:
- 0000 0000
- 0040 0000
- 0080 0000
- 0010 0000
- 00FF FFFF
- 0140 0000 (Start of Lynx Kernel)
- 00FF FFFF
- 001C 0000
- 0400 0000
- 0080 0000
- 0140 0000 (Start of Lynx Kernel)
- 0000 0000
- 0200 0000
- 001C
- 0417 FFFC
- 0400 0000
- 0800 0000
- 0C00
- 1234 5678 (hexadecimal address)
5 CVC Control and CAMAC Resources

The control and CAMAC resources are accessible from CPU and VDB.

5.1 Control and Status Register CSR, 2nd CSR

The CSR can be accessed from both VDB and CPU (long word access only). The CPU CSR address is hex. 041B E6C0, the VDB CSR address for ELTEC E-6 and crate no. 1 is hex. F03B E6C0. Multiple processing is supported by a second CAMAC cycle which can be accessed using address space hex. 041E 0000 to 041E FFFC. The corresponding second CSR address is hex. 041B E4C0.

**Note: The control register and status register have the same address.**

Fig. 4: Layout of Control Register (CR)

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>07</th>
<th>06</th>
<th>05</th>
<th>04</th>
<th>03</th>
<th>02</th>
<th>01</th>
<th>00</th>
</tr>
</thead>
<tbody>
<tr>
<td>Function</td>
<td>F</td>
<td>B</td>
<td>E</td>
<td>G</td>
<td>H</td>
<td>N</td>
<td>R</td>
<td>V</td>
</tr>
</tbody>
</table>

**Note: After reset or power up all bits of the control register are cleared.**

Fig. 5: Layout of Status Register (SR)

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>09</th>
<th>08</th>
<th>07</th>
<th>06</th>
<th>05</th>
<th>04</th>
<th>03</th>
<th>02</th>
<th>01</th>
<th>00</th>
</tr>
</thead>
<tbody>
<tr>
<td>Function</td>
<td>T</td>
<td>P</td>
<td>M</td>
<td>J</td>
<td>K</td>
<td>I</td>
<td>Q</td>
<td>X</td>
<td>F</td>
<td>B</td>
<td>E</td>
<td>G</td>
<td>H</td>
<td>N</td>
<td>R</td>
<td>V</td>
</tr>
</tbody>
</table>

Abbreviations in the tables above:

| V | CVC as slave. VDB interrupt bit. If set to 1, an IRQ for VDB master is set |
| R | Write only RESET bit. If set to 1, the CVC module will be resetted |
| N | Enable NVRAM write access |
| H | CPU HALT bit. If set to 1, the CPU will go to HALT state |
| G | Enable readout of Q, X response together with CAMAC data in single read cycle access |
| E | Disable bus error signal to CPU (for test purposes only) |
| B | VDB master block transfer enable |
| F | General purpose flag bit or SDRQ bit SCSI controller |
| X | Read only, X response bit. If 1, here was a CAMAC X response |
| Q | Read only, Q response bit. If 1, here was a CAMAC Q response |
| I | Read only. If 1, the CAMAC inhibit is set |
| K | Read only. The interrupt is set from another VDB slave |
| M | Read only. The CVC is in master mode |
| J | Read only. Boot jumper is on. See board description. |
| P | Read only. General purpose status bit of the extension port |
| T | Read only. CVC has VDB terminator on board |
5.2 CAMAC Interface

The CAMAC interface contains address decoder, NAF (N=station, F=function, A=sub-address) register, NAF decoder, sequencer and CAMAC drivers. Other crate controllers are not allowed together with the CVC in the same CAMAC crate. CAMAC data is clocked into the CAMAC Read Register CRR in the middle of the S1 signal. The CVC occupies the N=24 and N=25 CAMAC stations.

5.2.1 CAMAC N, A, F address space

The valid CAMAC address begin with N(1)F(0)A(0) hex. 04180800 and ends with N(24)F(31)A(15) hex.0418C7FC. Some additional addresses are decoded for CAMAC Initialize, Clear and Inhibit functions.

5.2.2 CAMAC NAF Register.

Fig. 6: CAMAC NAF Register.

<table>
<thead>
<tr>
<th>Address Bit Number</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>09</th>
<th>08</th>
<th>07</th>
<th>06</th>
<th>05</th>
<th>04</th>
<th>03</th>
<th>02</th>
<th>01</th>
<th>00</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAF Register</td>
<td>N</td>
<td>N</td>
<td>N</td>
<td>N</td>
<td>N</td>
<td>F</td>
<td>F</td>
<td>F</td>
<td>F</td>
<td>A</td>
<td>A</td>
<td>A</td>
<td>A</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

The CPU address bus bit A2 to A15 are connected to CAMAC NAF register, they correspond to CAMAC A1-A8, F1-F16, N1-N16 respectively. The content of the address bus is written to the NAF register at the beginning of a CAMAC cycle with the CPU address strobe (AS*) signal.

5.2.3 CAMAC Standard mode

The CAMAC standard mode is a 1 µs CAMAC cycle. The acknowledge to the CPU or to the VDB is send at the end of the cycle. The standard CAMAC can be selected with hex. 04180800..0418FFFC addresses. The data is read in the middle of the CAMAC S1 strobe.
5.2.4 CAMAC Short mode
The CAMAC short mode is a 600 ns CAMAC cycle, which ends after the CAMAC S1 signal is negated. The CAMAC short mode can be accessed from CPU only over the address space hex. 04190000..0419FFFC. The CPU needs only 100ns to trigger the CAMAC short cycle. The acknowledge to the CPU is send immediately over the synchronous termination (STERM*) signal. The CAMAC short mode is useful for writing or reading of great data blocks to/from CAMAC modules. The data read with short cycle is shifted one CAMAC Word (24 bit) to the right.

Fig. 7: reading data with successive short CAMAC cycles

The first data word (old DATA) is the data word from the previous CAMAC cycle and has to be ignored. During the read cycle CAMAC 2 DATA 1 is read, during the CAMAC 3 the DATA 2 is read and so on. To read the data corresponding to the cycle CAMAC n the dummy CAMAC read cycle must be send, or the CAMAC Read Register CRR have to be accessed.

5.3 CAMAC READ Register CRR
The CAMAC data can be read separately from the CRR without triggering the CAMAC cycle. The CRR can be accessed from the CPU only with address hex. 041A0000. The CPU read cycle duration for the CRR is 100 ns. The CRR is updated with new CAMAC data in the middle of the CAMAC S1 strobe. The data word read from the CRR is 32 bit wide, the bits 24-31 are read as zero. The X and Q response, if enabled with CR bit no. 04, can be read as data bit no. 30 and 31 respectively.

5.4 CAMAC Auxiliary Port Connector (ACB)
All LAM's and coded N signals (N16, N8, N4, N2, N1) have to be connected between the CVC and a Dummy Crate Controller over the ACB connector. The ACB is a 40 pin flat cable connector placed at the rear side of the CVC module.

5.5 CAMAC X and Q Response
The CAMAC X and Q response is memorized in two separate registers. One for the CPU CAMAC cycle and the other for the VDB-slave CAMAC cycle. The X and Q is available from the SR bit no. 8, 9 respectively. If enabled (CR bit no. 04 set to 1), X and Q can be read together with CAMAC data word. Bit 31 of the CAMAC data word corresponds to Q and bit 30 to X.
5.6 CAMAC Functions (Z, C, I)
There are special CAMAC NAF’s for the three following functions:

- **CAMAC INIT (Z)** is activated by addressing hex. 0418E6A0 or N(28)F(26)A(8). The INIT function executes a CAMAC cycle with B, S1, S2 and Z signals active. It activates the CAMAC INHibit line too.

- **CAMAC Clear (C)** is activated by addressing hex. 0418E6A4 or N(28)F(26)A(9). It executes a CAMAC cycle with B, S1, S2 and C signals active.

- **CAMAC INH (I)** line is set to active state by addressing hex. 0418F624 or N(30)F(26)A(9). Addressing of hex. 0418F6A4 or N(30)F(24)A(9) clears the inhibit. The INH function doesn't generate any CAMAC cycle.

5.7 CAMAC LAM Buffer (CLB)
The 24 bit LAM (Look At Me) buffer can be accessed from the CPU or the VDB over the address hex. 041C0000. The bit no. 1 corresponds to LAM from the station N1. If the LAM is active, the corresponding bit in the CLB is set to 1. The data bit no. 1 (D0) is connected to the interrupt controller if a 0 ohm resistor LM1 is placed on the CVC board. The sum of LAM (SLM) instead is connected to interrupt controller when SMD resistor SLM is soldered at the CVC board (see CVC board layout). The LAM1 or SLM can be connected at interrupt level 4 and generates the interrupt vector no. hex. 6C.

Fig. 7: LAM Connection DUMEX <> CVC
6 VSB Differential Bus (VDB) Interface

The VME Subsystem Bus (VSB) is a multiplexed 32 bit wide address/data bus. While the bus protocol is asynchronous, both address and data phase have to be acknowledged separately from the VDB slave. A timeout occurs if one of the acknowledge signals doesn’t arrive until a specified time (25µs for the CVC). The VDB is used for connecting CAMAC, FASTBUS and VME crates over distances up to 50 m. The VDB protocol uses only six of the VSB control signals: PAS*, WR*, ASACK, DS*, ACK, IRQ. The VDB is a single master bus. At the CVC the crate number is decoded with address bits AD21 to AD24. The valid VDB slave crate numbers are C=1 to C=15. Crate C=0 is used to switch to VDB master mode. The crate number can be selected with a switch at the front panel of the CVC. Data transfer size over the VDB is 32 bits parallel (long word) only.

6.1 VDB Interrupt

The VDB interrupt from a CVC-slave for a VDB master is set when the Control Register bit no. 1 is set to 1. The VDB interrupt for a CVC as master is connected to the interrupt logic and to the SR bit no. 1.

6.2 VDB Block Transfer

For the CVC as slave, the block transfer is always enabled. The whole CVC slave memory (1.5 Mbytes) can be accessed via VDB with Block-Transfer. The VDB address is send only once at the beginning of the Block-Transfer. At the CVC master mode the block transfer has to be enabled with CSR bit no. 7 (BT_EN) set to 1. The CPU have to access the VDB interface for required word count. After the last transfer the BT_EN must be set to zero. After RESET and power up the VDB-master block transfer is disabled.

6.3 VSB Differential Bus (VDB)

The VSB differential Bus can be connected to CVC over front panel 96-pin VGA connector. The differential cable allows distances up to 50m. Up to 15 crates can be accessed from one VDB master module.

6.4 CVC as VDB Master

After selecting the crate no. 0 and RESET (or power up) the CVC is set to Master mode. The CVC as VDB-master sends to the VDB 24 address bits (bit no. 2-25), the rest is set to zero at the VDB interface.

Fig. 8: Address bit Layout of CPU side input to VDB Interface

<table>
<thead>
<tr>
<th>Address Bit Number</th>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>Function</td>
<td>X</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>1</td>
<td>0</td>
<td>S</td>
<td>C</td>
<td>C</td>
<td>C</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>E</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Address Bit Number</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>09</th>
<th>08</th>
<th>07</th>
<th>06</th>
<th>05</th>
<th>04</th>
<th>03</th>
<th>02</th>
<th>01</th>
<th>00</th>
</tr>
</thead>
<tbody>
<tr>
<td>Function</td>
<td>N</td>
<td>N</td>
<td>N</td>
<td>N</td>
<td>F</td>
<td>F</td>
<td>F</td>
<td>F</td>
<td>F</td>
<td>F</td>
<td>A</td>
<td>A</td>
<td>A</td>
<td>A</td>
<td>A</td>
<td>0</td>
</tr>
</tbody>
</table>

Abbreviations: see next page
CAMAC Crate Controller with VDB Differential Bus, GSI Darmstadt, Jan Hoffmann

Fig. 9: Address bit Layout of CPU side output to VSB cable

<table>
<thead>
<tr>
<th>Address Bit Number</th>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>Function</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>S</td>
<td>C</td>
<td>C</td>
<td>C</td>
<td>C</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>E</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Address Bit Number</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>09</th>
<th>08</th>
<th>07</th>
<th>06</th>
<th>05</th>
<th>04</th>
<th>03</th>
<th>02</th>
<th>01</th>
<th>00</th>
</tr>
</thead>
<tbody>
<tr>
<td>Function</td>
<td>N</td>
<td>N</td>
<td>N</td>
<td>N</td>
<td>N</td>
<td>F</td>
<td>F</td>
<td>F</td>
<td>F</td>
<td>F</td>
<td>A</td>
<td>A</td>
<td>A</td>
<td>A</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Abbreviations used in figures 8 to 11

<table>
<thead>
<tr>
<th>If CAMAC is selected</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
</tr>
<tr>
<td>N</td>
</tr>
<tr>
<td>0</td>
</tr>
<tr>
<td>F</td>
</tr>
<tr>
<td>S</td>
</tr>
<tr>
<td>C</td>
</tr>
<tr>
<td>E</td>
</tr>
</tbody>
</table>

6.4.1 CVC VDB Master Address Space

The VDB master interface is located in the address space from hex. 0800 0000 to 0BFF FFFC (see CVC Addressing Overview on page 6).

The VDB master interface can access 64 Mbytes of VDB address space. Sixteen crates times 2 Mbytes equals 32 Mbytes, the S bit doubles this space.

6.5 CVC as VDB Slave

After selecting the crate number 1 to 15 and RESET (or power up) the CVC set to Slave mode. Addressed from VDB the CVC decodes the 23 address bits (bit no. 2 to 24) the others are ignored. The address bit layout is as follows:

Fig. 10: Address bit Layout of VDB side input to VDB Interface

<table>
<thead>
<tr>
<th>Address Bit Number</th>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>Function</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>C</td>
<td>C</td>
<td>C</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>E</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Address Bit Number</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>09</th>
<th>08</th>
<th>07</th>
<th>06</th>
<th>05</th>
<th>04</th>
<th>03</th>
<th>02</th>
<th>01</th>
<th>00</th>
</tr>
</thead>
<tbody>
<tr>
<td>Function</td>
<td>N</td>
<td>N</td>
<td>N</td>
<td>N</td>
<td>N</td>
<td>F</td>
<td>F</td>
<td>F</td>
<td>F</td>
<td>F</td>
<td>A</td>
<td>A</td>
<td>A</td>
<td>A</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Abbreviations: see table on this page
The CVC as a slave occupies 2 Mbytes (hex. 00000000 to 001FFFFF) of address space at the VSB Differential Bus (VDB). The crate number offset has to be added to it: e.g. for crate no. 1 the address space hex. 00200000 to 003FFFFF is active. This address space is translated to the CVC internal address space of (hex. 04000000 to 041FFFFF). The max. 1.5 Mbytes RAM, CAMAC, CSR and CLB can be accessed from the VDB. The VDB slave interface allows data block transfer.

6.5.1 VDB Interrupt Handling

The CVC Interrupts are connected to the VSB Interrupt controller in the VDB. The VSB interrupt controller is connected to two LED's: the front panel (信号灯) LED and the VDB LED (VIRQ).

The VDB Interrupt controller translates the interrupt vector number to the interrupt controller of the CVC. The interrupt controller generates the interrupt signal to the CVC.

<table>
<thead>
<tr>
<th>Transceiver</th>
<th>Interrupt Controller</th>
</tr>
</thead>
<tbody>
<tr>
<td>VSBI</td>
<td>D0 (V)</td>
</tr>
<tr>
<td>M_VSB_IRQ</td>
<td>D11 (K)</td>
</tr>
<tr>
<td>S_VSB_IRQ</td>
<td></td>
</tr>
</tbody>
</table>

Abbreviations: see previous page.
6.5.2 VDB Slave Addressing

The internal resources of the CVC reachable from the VDB side.

The address select bits no. 30, 27, 26 are set to 0 0 1 at VDB slave interface. The crate number address offset has to be added to the addresses shown below.

Example: For the internal CVC address hex. 04180800 the VDB address from the ELTEC E-6 for CAMAC crate no. 1 is hex. F0380800.

Table 2: VDB Slave Addressing Overview

<table>
<thead>
<tr>
<th>Source or Destination</th>
<th>Address (hexadecimal notation)</th>
<th>Long word (LW), Word (W) or Byte (B) Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>VRAM</td>
<td>RAM area accessed via the VDB slave interface</td>
<td>0000 0000</td>
</tr>
<tr>
<td>CAMAC</td>
<td>standard mode (1µs cycle)</td>
<td>0018 0000</td>
</tr>
<tr>
<td>CSR</td>
<td>Control and status register</td>
<td>001B E6C0</td>
</tr>
<tr>
<td>CLB</td>
<td>CAMAC LAM buffer</td>
<td>001C 0000</td>
</tr>
</tbody>
</table>
7 CVC Internal Resources

7.1 Serial I/O and Timer
The MC68C681 serial I/O (SIO) IC is used on the CVC for terminal and host communication. The connector for the SIO is placed at the front panel. The pin layout of it is: 1,6 not connected. 2,5,9,10 GND. 3,4 outputs for the terminal and host. 7,8 Inputs for the host and terminal. The base address of the SIO is hex. \textit{0C000000}. The access is 8 bit wide, SIO is able to supply two interrupt sources: SIO interrupt level 2 and TIMER interrupt level 6.

7.2 Cheapernet Interface
The ELTEC IPIN interface is used at the CVC as cheapernet interface. The IPIN is connected to interrupt level 3 of the CVC interrupt controller. The base address of the IPIN is hex. \textit{0C010000}.

7.3 Real Time Clock
The real time clock has a base address of hex. \textit{0C020000}. A data word is 4 bit wide, the 4 most significant bits of the readable byte are set to 0.

7.4 Interrupt Controller
The CVC interrupt controller can be accessed over two addresses hex. \textit{0C040002} for an interrupt source buffer and hex. \textit{0C040003} for interrupt mask register. Both are 8 bit wide and the source buffer is read only. The interrupt sources are:

After RESET or power up all mask bits are cleared and all interrupts are disabled. Timer and ABORT interrupts are edge sensitive, the others are level sensitive.
7.5 SCSI Controller

The SCSI controller is based on the AMD33C93 chip its address is hex. 0C036000. A detailed description of the SCSI bus can be found in the ANSI K3T 9.2 specification. The internal registers of the AMD33C93 are 8 bit wide. The SCSI controller is connected to the CVC interrupt level 5, the interrupt controller supplies the interrupt vector no. hex. 6D. The SCSI flat cable must be terminated at both ends. The SCSI data buffer of 64 Kbyte can be accessed at fixed address hex. 0C035000 by word access after setting the address counter at the address hex. 0C037000. The SCSI DBA (Direct Buffer Access) mode is enabled by setting the F bit (no. 07) of the control register CR at address hex. 041BE6C0.
8 MC68030 CPU Logic

Note: For proper operation of the CVC terminate VDB (terminator board plugged into first and last module in via VDB connected chain of CVCs)

8.1 Arbitration Logic

8.1.1 CVC as Slave
The address cycle of the valid VDB transfer begins the arbitration cycle between the VDB interface and the CPU. After the CPU has finished the last access the VDB-interface can execute the data cycle. Cheapernet IPIN has lower arbitration priority as VDB.

8.1.2 CVC as master
In this case the arbitration is done between the cheapernet IPIN and the CPU. No VDB arbitration is needed.

8.2 Time Out and Reset Logic
The time-out occurs while addressing non-existing addresses. The CVC time-out is set to 25 us. After that the BERR* signal is send to the CPU and a bus error exception occurs. The Bus Error signal to the CPU can be disabled (for test purposes) by setting the bit no. 05 of CR to 1.
9 Board Layout of CVC Version 4

Fig. 14: CVC Version 4, Standard CAMAC sized Board, Component Side
10 Board Layout of CVC Version 5

Fig. 15: CVC Version 5, CAMAC Standard sized Board, Component Side

```
Memory:
DMEM1  up to 16Mbytes dynamic RAM (DRAM 79A6)
MIM16  up to 16Mbyte static RAM (MIM16 3562)
```

```
all fuses 2 Amps
```
11 CVC Firmware

11.1 EPROM 1Mbit

Fig. 16: CVC EPROM (1Mbit)
11.2 CVC NVRAM 32 Kbyte

Fig. 17: CVC NVRAM

- Vector table: $400
- pRobe data
- pRobe stack
- Lynx OS parameters
- 1234 5678 hexadecimal address or data
11.3 CVC as Master
To set CVC to master mode select number 0 with crate number switch on front panel.

After power up or reset a wait loop of 5 seconds will allow the user to start pRobe monitor/debugger by pressing any key. If no key was pressed, the system will enter Lynx OS boot phase, executing a second wait loop allowing the user to stop boot procedure (by pressing a key) and enable command mode for changing parameters memorized in NVRAM.

To restart pRobe from Lynx OS reboot CVC by typing in the command \texttt{reboot -aN}, while in command mode the \texttt{F} command must be used.

11.4 CVC as Slave
To set CVC to slave mode select number 1 to 9 with crate number switch on front panel.

After power up or reset the pRobe monitor/debugger will start. The CVC can be reset remote via VSB from VSB master. This is done by writing 2 into CSR. It is possible to start any program from the VSB master. The remote start routine loop must check two addresses in memory, which are accessible from terminal or via the VSB cable. These two addresses are hex. 100 000 and hex. 100 004 in local memory. The first location should contain the start address of the user program to be started, the second location must contain the string \$\text{ICECAFFE}.

Lynx OS can be remotely stared (start address of Lynx OS is hex. 20) by typing in the command \texttt{go 20} from terminal.
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