The General Purpose Data Acquisition System MBS at GSI (and elsewhere)

PCI Express based Systems
Data transfer via Fibers
Custom Hardware
FEBEX2/3: Pipeline ADC Front End Board

FEBEX2: 8 ADC channels, 60MHz sampling rate, 12 bit resolution (60/12)
FEBEX3: 16 ADC channels, 60MHz sampling rate, 12 bit resolution (60/12) and 50/14

Purpose: Provide fast “digital electronics” to MBS community.
Filter “continuous” data streams from ADCs with respect to trigger windows.
In most case Pulse Shape Analysis (PSA: E, t) required.
EXPLODER1/2A

EXPLODER1: 32 LVDS input pairs
EXPLODER2A: 64 LVDS input pairs

Purpose: Provide a connection to all detector systems with LVDS outputs (Nxyter, GET4). Filter “continuous” data streams from detectors according to trigger windows.
FEBEX2
PEXOR: Front End Data Collector

4 SFP Fiber pairs each 2 Gbit/s to connect 4 x 256 front end boards at maximum

after 10/8 coding: 200 MB/s payload speed per SFP

4 Lane PCI Express > 600 MB/s FPGA -> PC DRAM payload speed
PEXOR-FEBEX2 Connections

Connection via:
- Fiber
- Copper cable
- Copper backplane

FEBEX: id 0
- FPGA
- CLK IN
- TRIGGER I/O

FEBEX: id 1
- FPGA
- CLK IN
- TRIGGER I/O

FEBEX: id 2
- FPGA
- CLK IN
- TRIGGER I/O

PEXOR
- FPGA
- TRIG. REG. I/O

GOSIP
PEXOR-TRIXOR-FEBEX Test Setup
(FEBEX not shown)
Traces from GO4 <- MBS <- PEXOR <- FEBEX
Star – versus Chain topologies between frond-ends and concentrator/readout boards:

Star:   Easy transfer protocol, limited number of frontends, hubs needed
Chain:   (More) complicated transfer protocol, highly scalable in size and speed.

GOSIP:
supports data transfer between PEXOR and FEBEX / EXPLODER (front-ends )for systems of sizes between
1 front-end and 1024 front-end cards. For data speed optimization, each front-end is equipped with two SFPs.
See topology in previous transparency, see GOSIP protocol below.

GOSIP supports Chain Initialization of all four PEXOR chains. During initialization each front-end gets a unique
module id, starting from 0 with the front-end closest to the PEXOR,

GOSIP supports Transparent Mode (read and write access) for slow control and setup issues from PEXOR
to each frontend with a speed of ~ 100K accesses/s:

A r/w request is send from the PEXOR upstream to front-end 0. Each frontend examines if the request is for itself.
If yes, it passes the result (read: ack and data, write ack) downstream to the PEXOR. If the request is for
a different front-end the request is passed upstream to the next front-end in the chain. Due to the chain topology chosen,
data coming downstream a chain, can pass all front-ends, via a FIFO, without intervention, until it reaches finally the PEXOR.

GOSIP supports Token Mode for fast data transfer from front-ends to PEXOR:

In token mode the readout toke is initiated by the PEXOR, which sends the token to the first front-end. This sends its data
packet down to the PEXOR and sends afterwards the token to the next front-end in the chain. The last front-end in the chain
sends the token after sending its data packet back to the token, which completes the transfer.
payload speeds of 4 times 200 MB/s have been measured.
Fast Token Data Transfer Options
Front-ends -> PEXOR

1) Wait for data ready mode: GOSIP waits until front-end declared data ready before sending content of data buffer 0/1. For triggered systems!

2) No wait Token: GOSIP sends data from data buffer 0/1 immediately on token arrival time downstream. Useful for “triggerless” systems!

FEBEX / EXPLODER FPGA (per input/ADC channel)
Fast Token Data Transfer Options
PEXOR -> PC DRAM / MBS

1) **Parallel token data sending** on for all connected front-end chains. Sequential DMA, initiated from MBS user readout function, from PEXOR to PC DRAM. Used for “small” data sizes.

2) **Sequential token data sending** for all connected front-end chains. Sequential DMA, automatically initiated by PEXOR FPGA from PEXOR to PC DRAM. Used for “big” data sizes. Limit is PC DRAM not PEXOR memory.
TRIXOR: - Identical functionality as TRIVA3/5/7

- Can be plugged in PCI Express or PCI slots. Takes only power.

- Works as master (trigger from input) and slave (trigger from trigger bus).

- Several TRIXOR and TRIVA can be interconnected via the trigger bus to compose synchronous bigger MBS systems.

- Communication with the TRIXOR via PEXOR and the Trigger Register I/O connector.

- Accepted trigger send a signal via the Trigger I/O connector to the PEXOR, which is then transformed into a PCI Express interrupt to notify the PC readout processor.
TRIXOR
TRIGGERING

1. Raw TRIGGER IN
2. Trigger Dead Time Locker
   Priority Encoder
   (VULOM, EXPLODER2A, LEVCON)
3. Accepted TRIGGER OUT
4. 4 bit encoded
5. Standard PC running MBS
   on LynxOS or Debian Linux

FEBEX Trigger and Clock Bus
2 in/out Common Clock for all FEBEX
2 in Physics and Sync Trigger
1 out Trigger request, OR from all FEBEX
FEBEX2/3 Features

- FEBEX2: 8 channels, FEBEX3: 16 channels
- 60 MHz, 12 bit, ± 1 V input signals
- ADC input circular buffer (per channel)
- Double signal trace buffer (per channel)

- I/O: IN (2): Physics trigger, sync. trigger
  IN:  Common clock (for hit timing)
  OUT: Common clock (dedicated FEBEX as clock master, external clock master)
  OUT: Trigger request from hit finder. OR from all channels (see below and next slide)

- Two hit finder (or self trigger) algorithms (3 step, trapezoidal filter)
- Dead time clear before readout (double trace buffer!)

- Data Output: Complete trace in trigger window and hit time (from common clock)
All features per channel:

- Enable/Disable Channel
- Enable/Disable Self trigger (hit finder)
- Enable/Disable Data reduction
- Set positive or negative input signals
- Even/Odd channel readout

- Set pre-trigger time (0 - 34 us, in nr. of ADC samples (1./60MHz := 16.7 ns )
- Set trace length (0 - 200 us, in nr. of ADC samples (1./60MHz := 16.7 ns )

- Select Self trigger method:
  a) 3 step
  b) trapezoidal filter, select one out of 4 different scanning frequencies
     60 -, 30 -, 15 -, 7.5 MHz
- Self trigger Threshold (in ADC counts, 0.5 mV steps)
FEBEX / EXPLODER Signal Input Stage

FEBEX / EXPLODER input stage implemented in FPGA for each ADC/Input channel:

Samples from ADC (60MHz)

Input ring buffer (2048 samples)

Data buffer 0 (12288 samples)

Data buffer 1 (12288 samples)

Input ring -, data buffer 0/1 for each ADC channel
Input ring buffer accepts ADC samples with the speed of the ADC without interruption
On occasion of a trigger, content of input buffer is copied with the speed of the ADC in a toggling mode into one of the data buffers

Length of input ring buffer defines maximum pre trigger window (see also next slide):
100 MHz: 20 us, 60 MHz: 34 us

Length of data buffer defines the maximum trace length (for hit finders/PSA):
100 MHz: 123 us, 60 MHz: 200 us

both Input ring buffer and data buffer sizes are a sensible choice. can be changed.
“Dead-time” free Data Acquisition with Trigger Windows

Trigger window adjustable from 1 sample to 12288 samples (FEBEX)

Note: - Trigger windows can be adjacent (no dead time)
- Avoid overlapping trigger windows by setting conversion time (minimum time between two triggers) to trigger window length
- Double data buffers 0/1 allow to release the system dead time before actual readout of data from FEBEX to PEXOR.
- Very large data sizes (data rates > 200 MB/s) might delay dead time release in a sense, that adjacent trigger windows (dead time free) are not possible in all cases. In this case the system is not anymore dead time free. This situation is also present in so called “trigger less” systems, when data rates produced in the frontends, exceeds the bandwidth of a transfer channel.
VULOM5 + SFPs
Connection VME <-> FEBEX / EXPLODER

VULOM5 SFP ADD ON

FPGA

FPGA

FPGA

VULOM5

VME

P1

P2

VME 2eSST: 150 MB/s
VULOM5 -> RIO4

4 SFP Fiber pairs
each 2 Gbit/s

after 10/8 coding:
200 MB/s payload speed
VULOM FEBEX/EXPLODER connections
Application with EXPLODER:

Readout of Nxyter chips/boards
- Running stable with MBS on PC with PEXOR,TRIXOR and EXPLODER / NXYTER.
- EXPLODER and Nxyter Synchronization with external clock (CLK IN).
- Reset of Nxyter clock with first hardware trigger to EXPLODER, armed after initialization.

Exploder + Nxyter front-end card  →  GEMEX
Test Hit Pattern of two Nxyter chips
Nxyter Internal Time Difference
(Nxyter 0 top, Nxyter 1 bottom)
Time Difference across two Nxyter chips
Channel (0-0, 7-7, 15-15)
ADC Nxyter, Channel 0, 7, 15

**Charge 01-27-21 2010-11-22 Analysis/Histograms/ADCCPCharge S 1 E 0 N 0 C 0**

- Entries: 236655
- Mean: 461.1
- RMS: 3.28
- Underflow: 0
- Overflow: 0
- Integral: 2.366e+05
- Skewness: 81.84

**Charge 01-27-21 2010-11-22 Analysis/Histograms/ADCCPCharge S 1 E 0 N 0 C 7**

- Entries: 236601
- Mean: 479.6
- RMS: 2.302
- Underflow: 0
- Overflow: 0
- Integral: 2.366e+05
- Skewness: 45.49

**Charge 01-27-21 2010-11-22 Analysis/Histograms/ADCCPCharge S 1 E 0 N 0 C 15**

- Entries: 236596
- Mean: 474.9
- RMS: 2.29
- Underflow: 0
- Overflow: 0
- Integral: 2.366e+05
- Skewness: 56.13
GEMEX (256 Detector Channels)

Project with Detector Lab GSI: 10000 channel GEM TPC
A real Experiment with
PEXOR, TRIXOR, FEBEX
The Search for Element 119, 120 at GSI

Connecting VME am PCI Express Systems
Accepted Trigger In

TRIXOR

PEXOR

LynxOS PC

Trigger Bus

TCP

640 Digital electronic channels
320 Detector channels

TCP

ADCs, Latches, …

TRIVA

RI03

VME

ancillary
(only if needed)

Event-Builder

LynxOS PC

Data Logging
Online Monitoring
Example Trace (pulse height: ~ 300 mV)

Trace length of 3000 := 50 us chosen to:

1) Cover rapid 120 decays within a single trace
2) VME dead time is always shorter than 50 us
3) Decent data size/rate
Example Trace (pulse height: \( \sim 15 \) mV)
FEBEX3, 640 Digital Channels
Structure for f_user.c, setup.usf and set_mo.usf identical for VME and PCI Express based systems.

MBS commands, messages, data logging, data monitoring identical for VME PCIe systems.

setup.usf needs only a few (static) changes (controller type, etc).

set_mo.usf needs usual customization for topology and node names.

f_user.c must be customized (as usual).