

First Silicon of the ALICE-TRD-ADC with 10b 10MSPS 5mW 0.1mm²

D. Muthers¹, R. Tielert¹ and V. Angelov²

¹Universität Kaiserslautern ²Universität Heidelberg

This report presents a short overview of the design of the Analog to Digital Converter for the Frontend Electronics of the ALICE Transition Radiation Detector [1] and some test results. The ADC is part of the TRAP1 chip, a mixed signal readout chip for the ALICE TRD, combining the discussed ADC together with a complete readout chain and four 120 MHz RISC processors. The final version of the TRAP-chip requires 21 ADC-channels, each with 10bit@10MSPS. Other ADC-designs offered this performance with 12mW of power consumption and 1.5mm² of area.

Among the different AD-Converter architectures the cyclic (algorithmic) architecture was chosen because it offers large improvements in terms of area and power for this application. The lowest-power 10b-ADCs recently reported have a power consumption around 1mW/MSPS. This design shows that it is possible to decrease the power consumption to 0.5mW/MSPS by consequent low power design and using a modern 0.18um CMOS process. The design allows a mixed-signal integration of ADCs and digital logic.

A cyclic converter works similar to the well-known pipeline structure. The quantization is performed sequentially bit after bit, while the signal "cycles" in only one stage. Fig.1 shows a block diagram of the ADC. The signal cycles in the amplifier block using switched capacitor techniques. As there are several ADCs on the chip, some parts like the

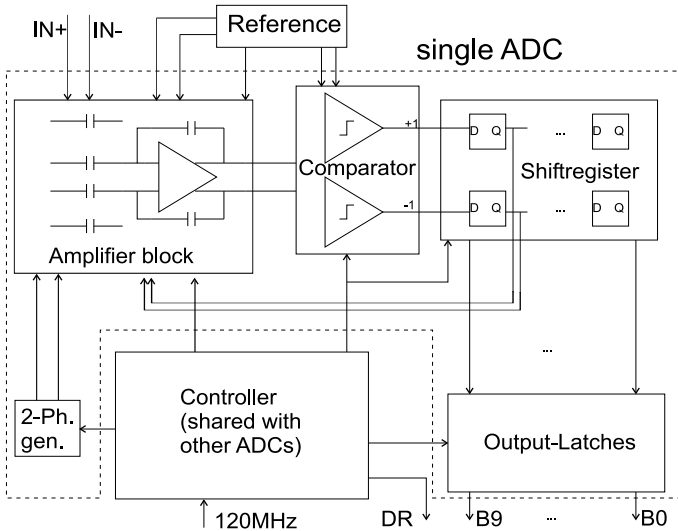


Figure 1: Block diagram of the cyclic ADC

controller are common for all converters, saving area and power.

A first version of this ADC was designed within 6 months. The testchip included three converters. Fig.2 shows a sampled sinewave of 100mVpp amplitude, having a RMS-error of 0.749 LSB. The measurements were performed with running digital part of the chip, using the same power supply for ADCs and logic. The results are very promising, since

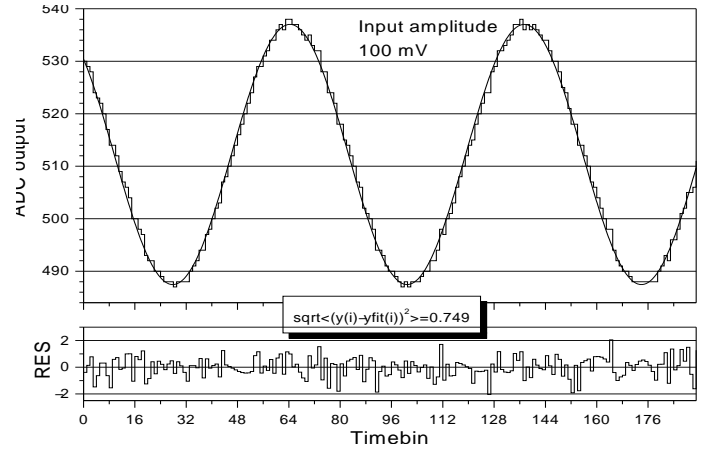


Figure 2: Measured 100mV sinewave

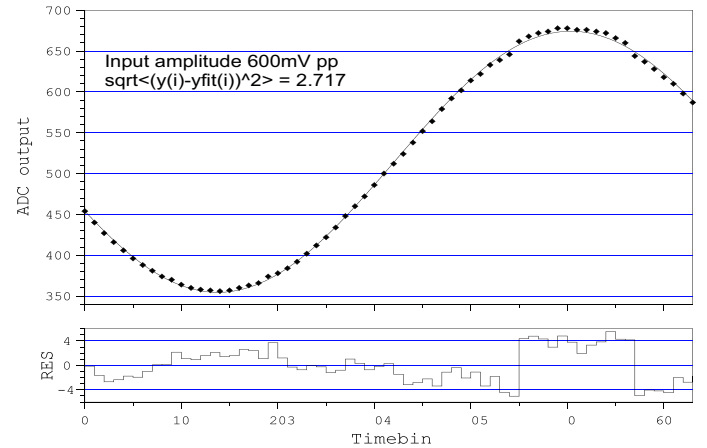


Figure 3: Measured 600mV sinewave

the remaining errors are fully understood and will be overcome in the next redesign. For larger signal swings like in Fig.3 linearity errors (steps) become visible, occurring at internal comparator thresholds. These errors are caused by parasitic coupling capacitances between the capacitors of the amplifier block, that were not fully recognized during layout design. Furthermore, even output codes appeared more often than odd ones due the timing of the internal autozero signal that started too early at the end of the last cycle. In the next redesign we will overcome these detected errors.

Summary: The first testversion of this cyclic ADC has been successfully implemented in the ALICE-chip. It offers large savings of area and power compared to other converters that are currently being used in similar experiments.

References

- [1] ALICE Transition Radiation Detector: Technical Design Report, CERN Sep. 2001