Front-end electronics for ALICE TPC-Detector

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The front-end electronics for the ALICE TPC to read out the charge detected by 570132 pads located on the readout chamber end-caps is here presented. The read-out chambers are multiwire proportional chambers with cathode pad read-out. The pads receive as the image charge of the signal on the anode amplification wires a signal with a fast rise time (less than 1 ns), and a long tail due to the motion of the positive ions. The signal is delivered on the detector impedance which varies between 3 pF to 12 pF. Therefore the front-end electronics must cope with different pad capacities. The electronics will be located in an area with limited access. High reliability is thus a concern. The circuit was developed in 0.35 μm CMOS technology.

The front-end electronics consist of a charge sensitive preamplifier/shaper, a 10-bit 10 MHz low-power ADC and an ASIC which contains a shortening digital filter for the tail cancellation, the baseline subtraction and zero-suppression circuits, and a multiple-event buffer [3]. The image charge induced on the TPC pads is amplified and integrated by a low input-impedance amplifier. It is based on a continously sensitive charge sensitive amplifier followed by a semi-gaussian pulse shaper of second order. The amplitude, which is different for the 3 different pad sizes, has a typical value of 7μA.

The Preamplifier/shaper for the ALICE TPC (Fig.1) is based on the design of the preamplifier/shaper for the NA45/CERES TPC. The main modifications concern:

- migration from the technology AMS CMOS 0.8 μm to the AMS CMOS 0.35 μm;
- optimization of the design to better fulfil the ALICE requirements;
- removal of the tail cancellation circuit that, in the ALICE design, is implemented in the digital ASIC.

This continuously sensitive design is particularly suitable for a detector with high occupancy. A peaking time of $\tau_s = 120$ ns and noise consideration ($<$ 1000 electrons) dictate a P-channel input transistor and a feedback resistance $R_F > 10$ MΩ. The feedback resistance R_F is realized by using a MOS transistor biased in subthreshold region. The MOS transistor MF establishes the DC path and continuously discharges C_F with a decay time $T_{decay} = C_F \times R_{ds}$ (MF).

The only practical way to realize such a high resistance in CMOS technology is by using the associated drain-source R_{ds}(MF) of a MOSFET transistor. A transistor operating in this area is very sensitive to process, temperature and supply voltage variations. To prevent or reduce these effects a Self-Adaptive scheme to bias the feedback transistor MF is used. The MOS-transistor Mzero is biased the same way as MF during the discharge of C_F. The Zero associated to the network Mzero-C1, adapts itself dynamically to accurately cancel the pole associated to the network CF-MF. There is also a benefit from the reduction of R_{ds}(MF) at high Qin, i.e. faster return to the baseline of the output of the CSA-shaper, without worsening the linearity of its conversion gain. In terms of noise requirements, the ALICE preamplifier/shaper fulfills the requirement with an ENC of less than 500 electrons for input capacitances between 3 pF and 17 pF. The response is linear ($<$ 0.2%) up to an dynamic range of 1.3 V with a peaking time around 120 ns. The gain of the preamplifier/shaper is about 7.8mV/fC. The total power consumption is 7 mW/channel.

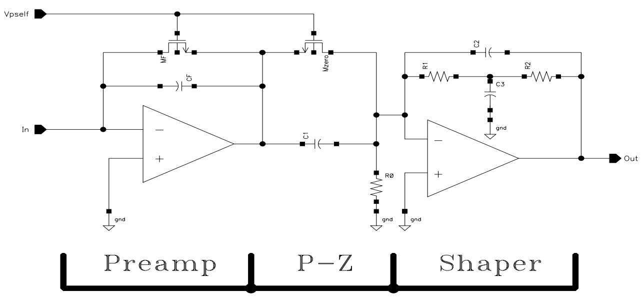

Figure 1: Schematic of the preamplifier/shaper chain.

The front-end electronics for the read-out for the TPC has been designed and fabricated with the AMS 0.35 μm CMOS process. The first prototyp is received and a first testing shows promising results. A new version is under development. The main change is the inclusion of a fourth-order filter to obtain a more symmetrical response to increase the double track resolution. The gain of the circuit will also be distributed towards the input to decrease the noise even further.

References

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