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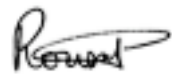
ACTAR Electronics and Data Acquisition

Dissemination level: *R/PU*Issued by: *SPhN/IRFU*Reference: *EURONS-D-J01-3.1*Status: *Final***Summary:**

A study was conducted to build an electronic system consistent with the ACTAR physics and instrumentation requirements. Given the different experimental methods a generic approach was developed and consistent with nuclear physics specifications. This final report describes the R&D program that will build the front end electronics and data acquisition system. The study included a methodology to be adopted to reach the goal with time-lines, description of the elements to be developed and deliverables. Also included are the procedures necessary to test the design by experiment.

28.11.2008

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EURONS- ACTAR JRA

Deliverable D-J01-3.1

Electronics and Data Acquisition system for an Active Target.

Within the ACTAR program three laboratories have joined forces to study a procedure and content for an R&D program that will build the front end electronics and data acquisition system for an active target detector. The study included also the procedures necessary to test the design by experiment. The study included a methodology to be adopted to reach the goal with time-lines, deliverables and description of the elements to be developed. We also have a budget study of the project. We consider it was not necessary to included here. In this study we were joined by a laboratory external to the JRA. Essentially this was because one of the initial members of ACTAR joined NSCL, MSU.

The project of providing ACTAR with an adequate front-end electronics and acquisition was undertaken by first studying the requirements for such a system against what is presently available. To highlight the findings we give below a short history of what the particle physics community has as possible solutions.

Electronic systems to read Track Projection Chamber have to measure the deposited charge and the arrival time of signals on the detector readout plane. Since the mid 1990's, work was done to improve TPC electronics to increase the number of pixels on the readout plane. It started with the NA49 and the EOS R&D program. It was materialized by the STAR (Solenoidal Tracker at RHIC) electronics [16] in 1996. Since the beginning of 2000, the only large size TPC built was the ALICE tracker for the LHC, where a complex processing system, different from STAR, was developed. It used PASA and ALTRA circuits [17]. Since 2004, two projects worked on the electronics of large size TPC. The EUDET program, founded by EU, works on the tracker for the future collider ILC and the neutrino experiment at TOKAI (T2K - Japan). For these projects more integrated electronics, associated with state-of-the-art ASIC [18] where developed to process analogue signals from the detector and a fast digitization based on pipeline ADCs and FPGAs with integrated processors. In the meantime IRFU, Saclay, with its know-how in mixed circuit conception to readout capacitive detectors and in data acquisition systems for physics experiments, has developed an electronic system and its integration for T2K. The system is well adapted to T2K. Nevertheless, in spite of its excellent assets (low power consumption, 72 integrated channels, gain and shaping time fully settable); it carries major disadvantages incompatible with future detectors, in particular for nuclear physics. It needs new technologies, an internal trigger system and fast readout architecture. Along with the two existing electronic systems (ALICE and T2K), there is no other electronic structure to give time and charge with adequate resolution.

An aspect of this project which is of import to mention is the need to build or have a generic front end electronics to cater for the different detector that the ACTAR physics and instrumentation program suggests. Further that specifications must be such to satisfy the very specific nuclear physics needs. To draw attention to these prerequisite they are listed below with attached explanations;

1. Present studies have been mainly limited to light nuclear systems. With the advent of powerful secondary beam accelerators, such as Spiral2 or the gas-stopper coupled to a post-accelerator at MSU, new opportunities will be offered in the medium to

Task T-J01-3: Electronics and data acquisition

heavy mass region. This implies the need for better resolution to resolve individual states in the higher mass nuclei. **This, in turn, implies a decrease of the pad-size, and hence an increase of the number of channels by one order of magnitude.** The front end electronics of the new system must allow a large number of channels to be captured per cm², ~25 channels/cm².

2. In the inverse kinematics of such experiments, the energy of the recoil particles varies over a very large energy range, for example protons or deuterons in the energy domain of 100 keV/nucleon to several tens MeV/nucleon. The incident heavy particles have a very high specific ionisation power as compared to higher energy light particles. **Therefore an unprecedented dynamic range is needed.**

3. The low energy recoil particles will stop within the detector gas. This implies the need of an internal trigger. **This is a new feature with respect to existing TPCs, and the associated trigger logics are a new development.**

4. The properties of the gas must be chosen essentially by the needs as target, and very diverse gases, not optimised for the detection, will be used, such as Hydrogen, deuterium, ^{3,4}He. This implies a very broad range of drift-times, and consequently **the sampling frequencies will have to be adjusted between 1 Mhz and 100 MHz to follow the drift of the particles.**

5. Considering the expected performances in terms of data rate and number of channels, new software must be developed, based on the framework used in particles physics. It will allow rapid development of test bench and part of data acquisition computer system.

To summarise we note that;

- A generic approach in the ASIC development including adjustable gains and discrimination per channel leading to a smart trigger must be employed.
- Development and test of an applicative software framework for the configuration, the acquisition and the data storage based on the new computer science technologies associated with NTIC (nouvelle technologie pour l'information et de la communication).

The program is called 'General Electronics for TPCs', GET.

1. THE GET PROGRAM

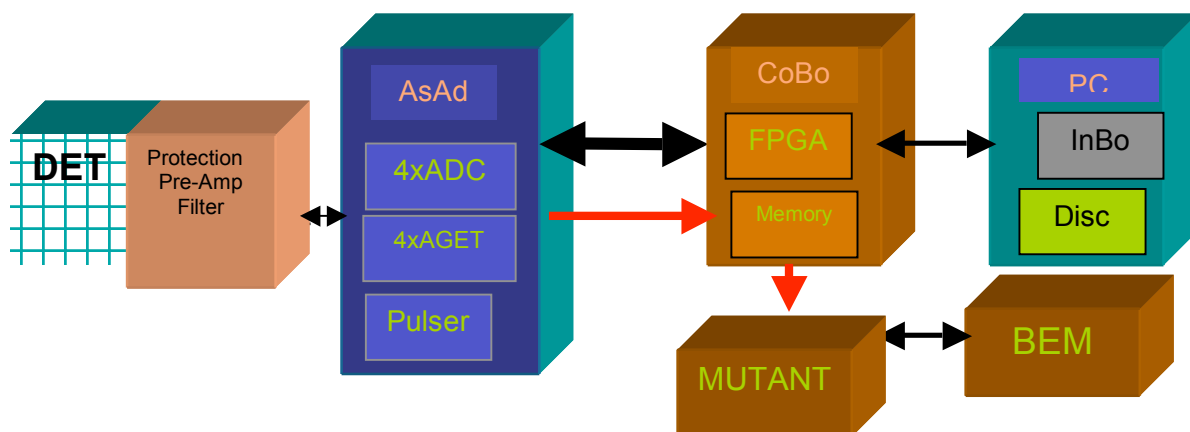


Figure 1.1

The basic hardware elements of the system to perform the experiments to be developed are shown in the figure 1.1. Pads of the detectors (DET) are the source. Each pad is electrically connected to a spark protection circuit followed by the preamplifier and filter stage (Pre-Amp & File). The output is fed into one of the 72 channels of the ASIC, AGET (Asic for GET). AGET must sample the incoming signal continuously at a given frequency (~1 to 100MHz) and has also to send logic signals to the trigger unit (MUTANT) when the set threshold is exceeded. Once the appropriate combination of signals is reached in MUTANT, a trigger and a calculated hit pattern is issued. This has to stop the input-reading of AGET and the ADCs on the front end board AsAd (Asic & ADc) will read the hit channels. Numeric data from 4x (AGET+ADC) are sent via copper cables to CoBo (COLlection BOard). Data reduction, time stamping and ordering as well as other more complex functions are performed in the FPGA and stored in a buffer Memory. Data is transferred on a fast optic link to InBo which resides on one of the acquisition PCs. Each CoBo fits 4 AsAd (4x4x72 channels) and each InBo fits 3 CoBo (3x4x4x72). So for a relatively large experiment 4 to 6 InBo are employed on two PCs. The data merging with other systems (spectrometers, particle detectors, etc) is accomplished using time-stamping where the internal clock of GET is synchronised to the external clock. The throughput in the system (14,000 channels) that is requested is at least 1 KHz internal triggers with a few percent dead-times for high pad occupation events. To allow for different gas amplification methods and different amplification zones of the detector a number of options are possible; the configurable external or internal pre-amp plus filter; the gain is adjustable per AGET by a factor of 100 from 100 fC with fine tuning per channel; the discriminators are set per channel; the peaking time must be adjustable from 50 to 1000ns. The time and charge resolutions will be better than 2nsec and 0.1% (at 130fC) respectively. Software control developed at IRFU/LILAS will be employed for the development stages and to operate, calibrate and adjust the system and protect the hardware. The French develops NARVAL system allows for data flow and run control [<http://informatique.in2p3.fr/?q=node/302>] will be employed.

2 METHODOLOGY

PARTNERS

Partner	
1	IRFU Saclay, France
2	GANIL, CAEN, France
3	CENBG, Bordeaux, France
4	NSCL/MSU, Michigan, US

The Partners of GET are listed above. NSCL/MSU will share the budget expenditure in GET and will not profit directly from the ANR budget.

CEA and IN2P3 have a great experience in the management of projects linked to the nuclear instrumentation. The internal organization of CEA and IN2P3 [PROJ1, PROJ2], sharing the same tools, are based on a system of project reference allowing to follow the rules of the AFNOR standard (FDX50-115 December 2001).

The organization of tasks is based on the Project Breakdown Structure (PBS+WBS) and a management plan based on the Organization Breakdown Structure and WBS.

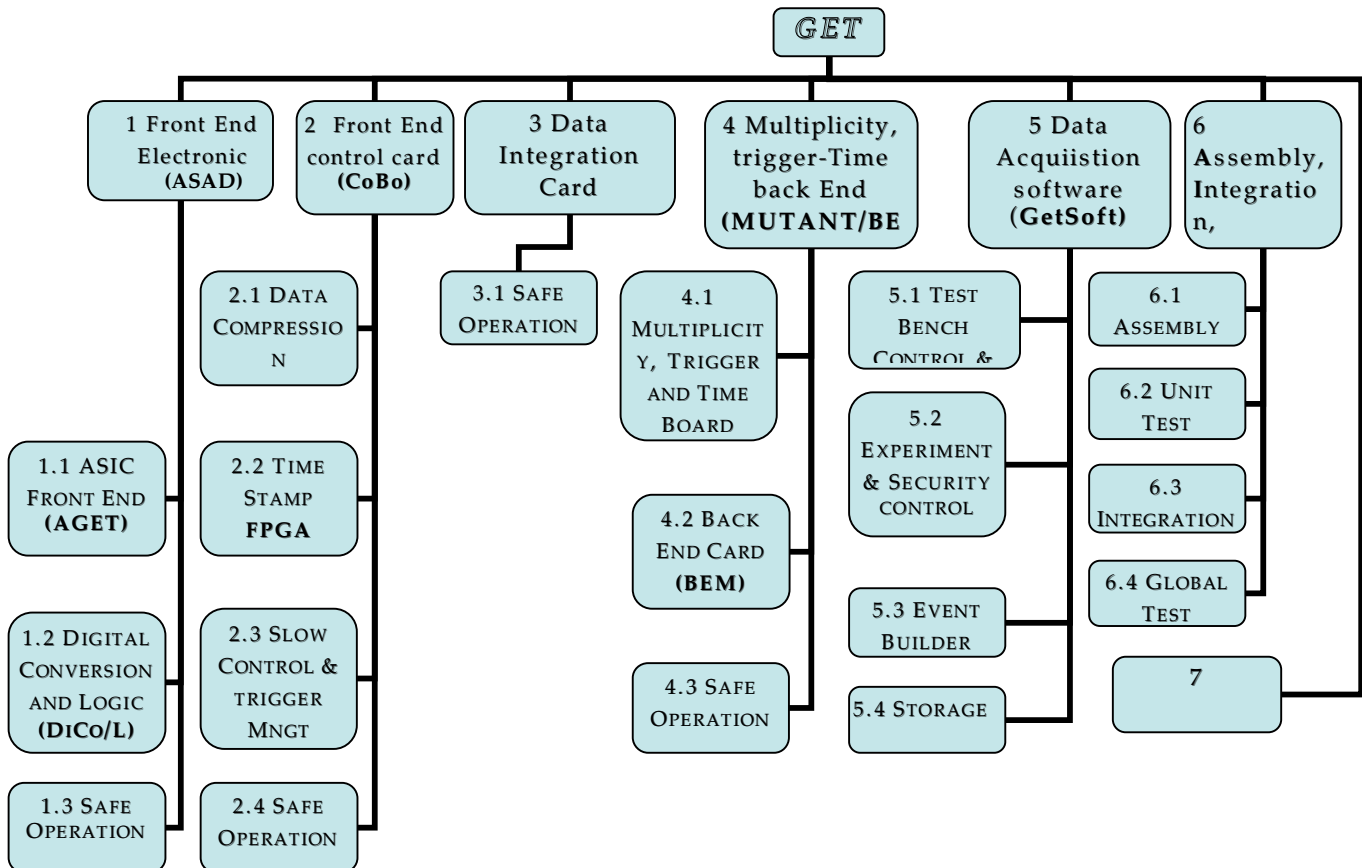
The scientific impact will be to perform experiments giving the nuclear physics community a lead in experimental physics with low energy detection and high luminosity. As for the technical impact, it will place the French community in a leading position in TPC oriented

Task T-J01-3: Electronics and data acquisition

numeric data capture. Further, the technical development will try and set standards and methodology for a large fraction of systems being introduced at SPIRA2.

3 PROJECT BREAKDOWN STRUCTURE

The aim of GET is to conceive a generic electronic system going from the front end to data storage, focusing on TPCs used for nuclear physics experiments.



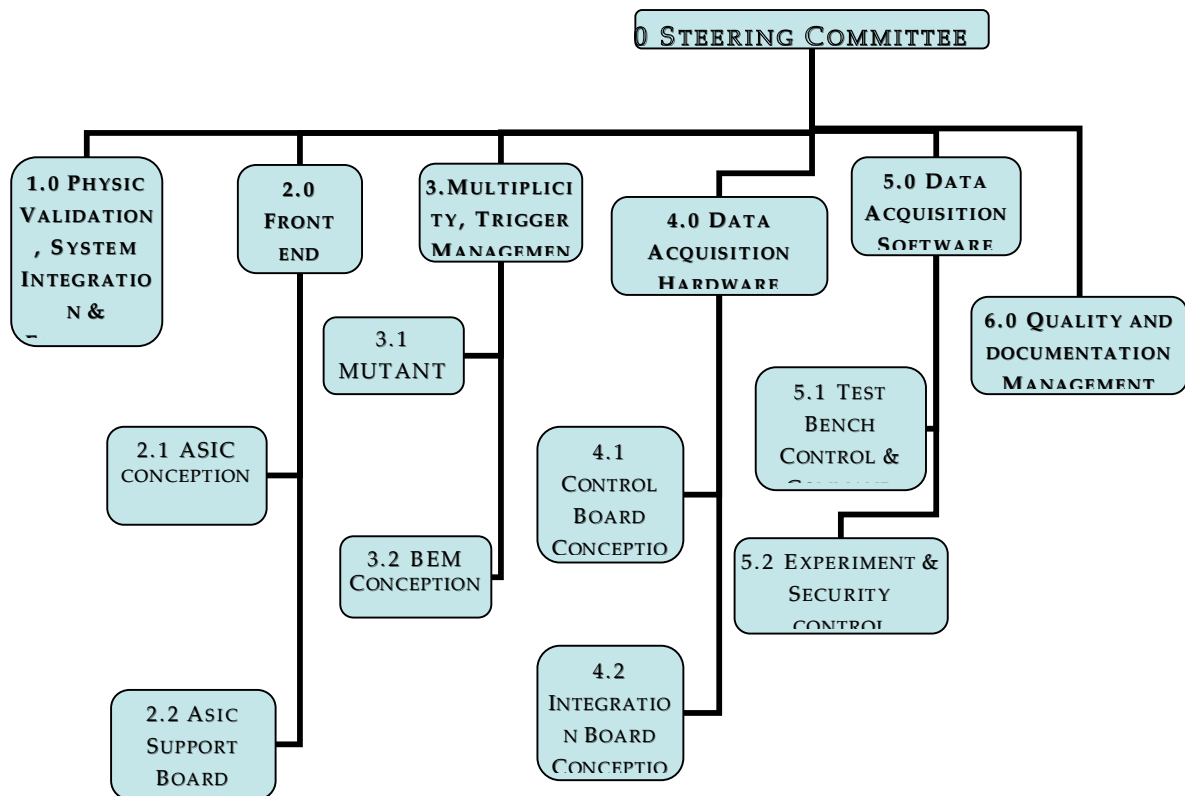
Task T-J01-3: Electronics and data acquisition

<u>Product id</u>	<u>Product Name</u>	<u>Description</u>	<u>INSTITUT</u>
PBS_7.0	Management	It pilots the technical aspect, costs, time schedule of the different tasks, report to the steering committee, and manage the "leftover" of the project. The group will have in charge the quality assurance, the interface management between tasks (WBS) and the documentation.	<u>IRFU,CENBG, GANIL,MSU</u>
PBS_1.0	Front end electronic	The front end board must integrate the AGET asic, the detector connection, digitization and power management. It could incorporate monitoring functions as temperature & power supply measurement.	<u>CENBG,IRFU</u>
PBS_2.0	CoBo	The board controls several front end board in term of configuration, monitoring, acquisition and data processing	<u>MSU, GANIL, IRFU</u>
PBS_3.0	InBo	The board controls and save data from several CoBo board. It manages optical link communication aspect.	<u>GANIL,MSU</u>
PBS_4.0	MUTANT/BEM	The board provides Time start to all other boards; manage the multiplicity algorithms and also the trigger input.	<u>GANIL,MSU</u>
PBS_5.0	GETSOFT	The Software is user friendly interface to control all the hardware for configuring, acquiring and storing data in an exploitable format.	<u>GANIL, IRFU</u>
PBS_6.0	Assembly, Integration & Test	It will provide all procedures to integrate and to test the complete system.	<u>CENBG, IRFU, GANIL, MSU</u>
PBS_1.1	AGET	Front end Asic	<u>IRFU</u>
PBS_1.2	ASAD	Support board for the front end	<u>CENBG</u>
PBS_2.1	Data Compression	Algorithm to acquire and to compress data (ADC control, zero suppression...)	<u>MSU</u>
PBS_2.2	Time Stamp	To provide a time stamp per event relative to time information	<u>MSU,GANIL</u>
PBS_2.3	Slow Control & Trigger	To configure all needed parameters before starting an acquisition. It waits about a trigger signal too.	<u>MSU,GANIL</u>
PBS_4.1	MUTANT	To handle multiplicity algorithm and send trigger signal to all CoBo boards.	<u>GANIL</u>
PBS_4.2	BEM	To Provide interface between trigger and the system.	<u>GANIL</u>
PBS_5.1	Test Bench C&C	Build a library to develop uniform testbench software all around board development.	<u>IRFU, GANIL</u>
PBS_5.2	Experiment and security C&C	Development of the final software for building experiment at GANIL and elsewhere it is needed.	<u>GANIL, IRFU</u>
PBS_5.3	Event Builder	Create a data format for all parameters and readout data.	<u>GANIL, IRFU</u>
PBS_5.4	STORAGE	Storage data in a SGBD or equivalent	<u>GANIL, IRFU</u>
PBS_6.1	ASSEMBLY	Prepare the assembly of the different module to prepare experiment	<u>CENBG,GANIL</u>
PBS_6.2	Unit Test	Test of each part of the system before launching an experiment	<u>CENBG,GANIL</u>

Task T-J01-3: Electronics and data acquisition

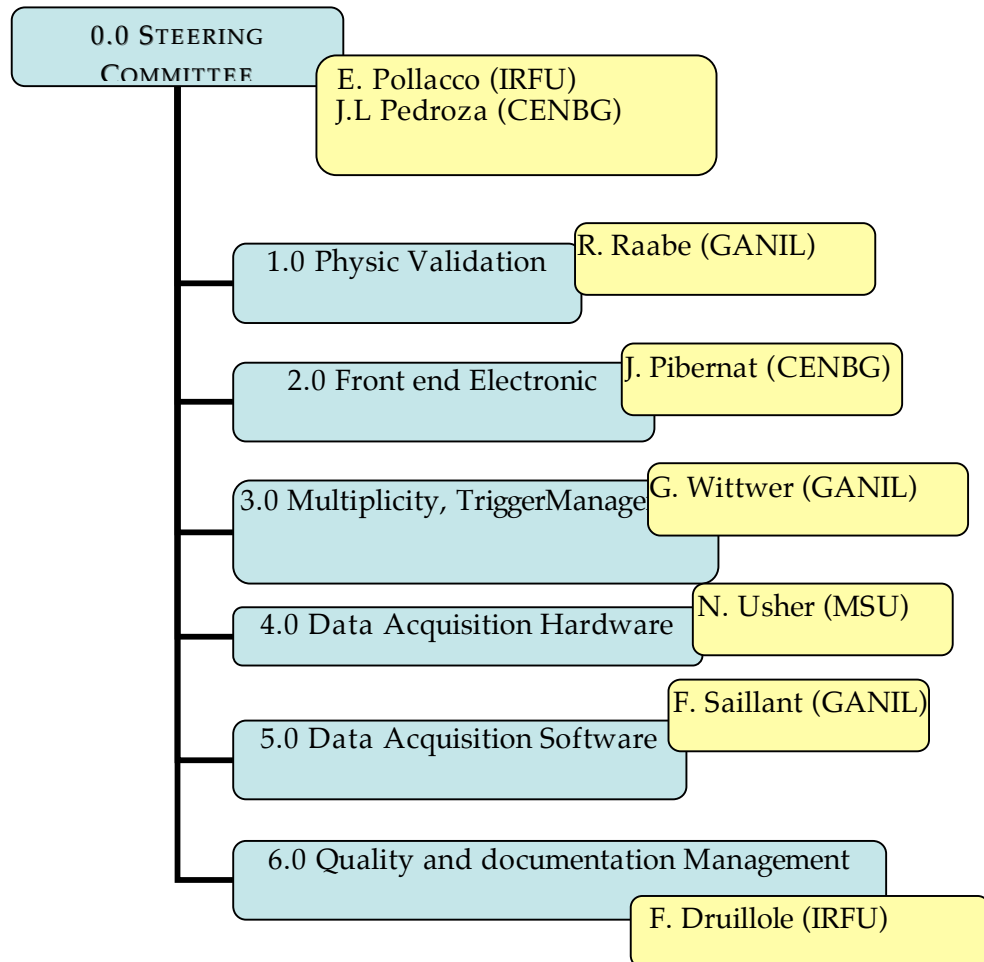
PBS_6.3	Integration	Integrate the system in situ for preparing the experiment	CENBG,GANIL
PBS_6.4	Global Test	Pre-check of the electronic system	CENBG,GANIL
19 products			

i. WORK BREAKDOWN STRUCTURE



b. COORDINATION DU PROJET / PROJECT MANAGEMENT

i. ORGANISATION BREAKDOWN STRUCTURE



ii. WBS 0.0 STEERING COMMITTEE

The Steering Committee is composed of 8 members: 1 physicist and 1 engineer from each partner.

The role of the Steering Committee (WBS_0.0) is the following:

1. Coordinate the other tasks
2. Coordinate the meetings
3. Report on expenses
4. Communicate with ANR
5. Write a Conceptual Design Report.
6. Coordinate the interfaces of the project.
7. Write an Interface Design Report.
8. From the tasks intermediate reports compile the Technical Design Report.

Task T-J01-3: Electronics and data acquisition

The management checks that tasks flows go smoothly (with proper management inside the tasks), that deliverables due by each task are ready on due time and that the communication between tasks is efficient. For this, meetings will be organized every 2 months (50% by videoconference) or more frequently when necessary.

The Steering Committee coordinates the interactions with all tasks. In others terms, it guarantees that all the interfaces of the project are well defined. It follows advices from task WBS 6.0 to perform quality assurance on each task and check the appropriateness of each product to the definition of the whole system. Its entire works are based on the works of the different tasks (WBS).

The Steering Committee also coordinates the interactions with outside partners such as future users, special requests for the GET system.

Deliverables of the management task are:

- Progress reports every 6 months.
- An intermediate report showing the expenses every year.
- A conceptual design report after six months.
- An intermediate Interface Design Report (T0+12).
- A final Interface Design Report (T0+36).
- An intermediate Technical Design Report (T0+12).
- A final Technical Design Report (T0+36).

C. DETAILED DESCRIPTION OF THE WORK ORGANISED BY TASKS

The tasks described below have the prime objective to build and check through experiments a prototype GET system to reproduce the required specifications. With reference to the (GANIL/SPIRAL2 & GSI/NuSTAR) physics described in sections 1 and 2, it is deemed that the experimental method, in conjunction with GET for data capture, is essential to reach the physics goals and to remain competitive in the field.

Apart from the general exceptional performance, (dynamic range, charge and time resolution, through-put bandwidth, etc within a multi system approach) we integrate other essentials design features (thermal constrains, mechanical layout, E-M immunity, scalable, thermal and tension secured, portable, automated calibration and performance stabilisation, costs and schedule modular etc) and options (plug & play, online debugging, user-oriented, part future-proof etc.) necessary for nuclear physics where reliability and malleability over large sequence of experiments is a premium.

i. WBS 1.0: PHYSIC VALIDATION, SYSTEM INTEGRATION AND EXPERIMENTS

• *Responsible*

Riccardo Raabe - GANIL

• *Objectives*

This task is central, and all partners are involved. Through WBS 1.0 the Conceptual Design for GET is drawn to reach the physics specifications. Further, it ensures throughout the project that the requirements are effectively implemented and validated. The task will provide the necessary framework, interfaces and experiments for the final prototype verification in nuclear physics measurements. At present time, two validation experiments are planned, to check the functionality of the GET electronics in the different configurations, for the measurement of a reaction and a decay process.

- *Detailed work program*

Implementation of the requirements for each TPC

The precise requirements on the performances of the GET electronics were formulated for the TPCs of next generation that are presently being designed. Also, the work was guided by the identification of physics cases leading to key experiments. The results constitute one of the outputs of the ACTAR JRA within the FP6 EURONS program.

The various TPCs have different specifications depending on the physics program pursued. For the GET electronics, we will consider, in first instance, the detectors developed by the partners in the present ANR:

- The new active target at the GANIL laboratory (physics case: reactions in inverse kinematics with the SPIRAL2 radioactive ion beams).
- The TPC at the MSU laboratory (physics case: heavy ion collisions).
- The TPC at the CENBG laboratory (physics case: two-proton emission and other exotic decay modes at the driplines).

We also take into account the interest and ideas expressed by other laboratories and research groups involved in the ACTAR JRA.

The specifications will be translated in a series of parameters to be implemented in each of the modules of the GET electronics (front-end, multiplicity-trigger, numeric data reduction, run and slow control). This takes place at the design level of each module. Role of the present subtask is to ensure that this is done correctly within each module and coherently across the different modules.

This is achieved by participating (at least one person in this task) in the regular meetings where the design and specifications of each module are discussed and decided. The minutes of the meetings and summary of decisions are the base for a first documentation, which is used as reference for the advance of the various designs. Regular communication between the persons in this task (by email, telephone and phone conference) is kept, to ensure a cross-check between the designs.

External reviewers will be used to help in the process. They will follow the progress of the single and overall design, collaborating with the task responsible in the evaluation. Expert from STFC Daresbury, GSI Darmstadt and KVI Groningen, who were involved in the ACTAR JRA, have been contacted.

No deliverable is associated with this step – the outcome is in the design study of each module.

Description of possible configurations of GET

The use of GET, as associated with a TPC and for a particular experiment, will be elaborated by the persons in this task. Each physicist will focus on the TPC of the corresponding laboratory; he will determine the electro-mechanical optimal parameter for a representative experiment or a set of experiments, according to the physics cases (as identified in the ACTAR JRA). The parameters will include the number of channels, dynamic range, cross-talk, trigger policy, sampling frequency, software robustness, data through-put, event-building and structure.

The deliverable is a report, in form of a “user guide”, where the configurations are presented. The document will serve as a set reference in the preparation of experiments.

Preparation and execution of test experiments

The prototype will be assembled for testing and final validation in nuclear physics measurements. We have identified two key experiments to test the main functionality of the GET electronics in very different configurations. The choice of the experiments has also been made in order to cover the two main physics cases considered for the applications with the GANIL/SPIRAL2 ion beams.

- Transfer reactions: $^{12}\text{C}(^8\text{He}, ^7\text{H})^{13}\text{N}$

Task T-J01-3: Electronics and data acquisition

This one-proton transfer reaction can be used to produce the unbound ${}^7\text{H}$ system. A measurement took place with MAYA [10]; in that occasion seven events were observed. The use of GET electronics, implemented in a MAYA-type active-target detector, will allow collecting a significantly larger statistics, to validate the observation of the ${}^7\text{H}$ ground state and its characteristics (its position, the surprisingly narrow width, its spin). A larger statistics (about one order of magnitude) will be achieved by a) an increase of the gas pressure in the target by a factor 2 or 3, and b) the increased geometrical efficiency for the detection of the recoil ${}^{13}\text{N}$ tracks, which identify the reaction channel. A higher pressure translates directly in a larger target thickness; however, the tracks of the recoil ${}^{13}\text{N}$ are shortened by the same factor. An increased density of detection pads, and thus readout channels, is then necessary to provide the resolution required for the identification of the recoil nuclei. Concerning the efficiency, the current limitations in MAYA (the tracks must span several pad rows) will be lifted thanks to the readout ensured by GET.

GET will be tested with respect to the high data throughput, dynamic range, noise threshold, at the highest sampling frequency.

- Two-proton decay studies:

In another experiment, the GET electronics will be tested in the case of radioactive decays. Two-proton radioactivity of e.g. ${}^{45}\text{Fe}$ is in competition with other complex decay modes like β -delayed 2 or 3 proton emission. The present version of the Bordeaux TPC [7] does not allow distinguishing these decay modes efficiently. In particular, if the projection of the proton traces on the detection plane overlap, the fact that the present version of the TPC has no flash-ADC like timing signals hinders the identification of these traces. The GET electronics will allow clearly identifying and distinguishing these decays.

Another problem resolved by the GET electronics is related to the data acquisition dead time. The implantation-type event of a 2p emitter (e.g. ${}^{45}\text{Fe}$) is followed closely in time by the radioactive decay. The test of the prototype electronics will allow verifying that the data through-put is fast enough to prevent loss due to an excessive dead time of the system.

Finally the test of the prototype will also allow to study whether problems due to rather different dynamical ranges between and implantation-type event and a decay event can be handled routinely.

In the two cases the GET electronics will be configured according to the document produced at step 2.

Deliverables of this step are: the reports of the tests and experiments (summary of logbooks and conclusions); where necessary, a revision of the “user guide” produced at step 2. Scientific publications will be prepared about the results of the experiments.

ii. WBS 2.0 FRONT-END ELECTRONIC CONCEPTION:

Sub-task : Asic Conception (AGET)

Responsible: Pascal Baron CEA/DSM/IRFU/SEDI/LDEF

Author: Pascal BARON, (IRFU/SEDI)

The LDEF of the CEA/DSM/IRFU/SEDI has in charge the design of the AGET asic. This laboratory has an expertise in the microelectronic domain through different projects in the fundamental physic research. The LDEF has designed the AFTER chip [AGET1] and is the ideal laboratory to study and realize the new powerful version of this chip. In this way,

Task T-J01-3: Electronics and data acquisition

this work will be achieved by the same designers of the AFTER chip optimizing therefore the success and the time of the operation.

As this chip is a one part of the GET electronic, its development phase will be coupled with the other parts of GET and therefore will imply a great cooperation between the different partners, especially for the definition of the requirements and in the validation of the prototype phase.

The goal

The goal of this task is to realize an upgrade of the AFTER chip by changing some specifications and by adding new functionality. These modifications are necessary to support the relative highest counting rate (10 kHz) and to participate to the definition of the trigger. These different points are:

In the Front end part level:

- Modification of the input charge range: 120fC, 1 pC or 10 pC, adjustable per channel. [Previously: 120 fC, 240 fC, 360 fC or 600 fC adjusted and common for all the channels]. This provides to the chip highest input charge coverage.
- Modification of the peaking time range: 16 values between 50 ns and 1 μ s. [Previously: 100 ns to 2 μ s]. The drift time of the TPC is faster than the one of the T2K TPCs. It permits also to gain silicon area needed to put a part of the additional features.
- Possibility to bypass the internal CSA and to enter directly to the shaper or SCA inputs. This will be useful in the case where a connection to an external CSA is needed (for topology or noise considerations).
- Auto triggering: one discriminator and one threshold (DAC) per channel. This new feature is important for the trigger generation and for the speed of the readout phase.
- Multiplicity output data: the chip will give a signal corresponding to the sum of the 72 discriminators outputs to form the trigger of level 1.

In the SCA and readout part level:

- Several mode of SCA read out: 128, 256 or 511 analog cells.
- Several mode of channel read out: hit channel(s), specific channels or all channels.
- Read out of the hit channel address.

These readout modes permit to support highest counting rate and to have a better pulse double resolution.

These novel functionalities will offer to the AGET chip a high versatility and will permit therefore to be used in a different environment with a high level of adjustment. A synthesis of the AGET requirements is reported in the table 1.

Parameter	Value	Parameter	Value
Power consumption	< 10mW / channel	Trigger	
Polarity of detector signal	Negative or Positive	Discriminator solution	L.E.D
Number of channels	72	Dynamic range	5% of input charge range
External Preamplifier	Yes	I.N.L	< 5%
Input dynamic range	120 fC; 1 pC; 10 pC	Threshold value	4-bit DAC / channel + (3-bit + polarity bit) common DAC
I.N.L of the charge measurement	< 2%	Minimum threshold value	\geq noise
Resolution (Charge range: 120fC; Peaking Time: 200ns; C_{in} < 30pF)	< 850 e-	Readout	
Peaking time value	50 ns to 1 μ s	Readout freq.	20 MHz to 25 MHz
Number of SCA Time bins	511	Counting rate	< 1 kHz
Sampling Frequency	1 MHz to 100 MHz		

Table A2.1: List of the AGET requirements

Development phase

There will be two phases: the design and the test phases.

Design Phase

The study and validation of the new design (architecture, schematic, simulation and layout) will be made by using the CAD software tools from CADENCE. The estimated time of the

Task T-J01-3: Electronics and data acquisition

global design is in order of 4 months. This time is shorter than usual (around of one year) since a great part of the design is already achieved and validated.

The chip will be manufactured in a 0.35 μm CMOS AMS process and will be received back 3 months after.

Test Phase

In parallel of the asic design, a test bench (hard & soft) must be build and ready for the prototype test. The relative short time of the asic prototype phase doesn't allow the possibility to use the GET system for this test. We will focus firstly on the test bench used for the AFTER chip. This system has been developed in the CEA/DSM/IRFU/SEDI and can be upgraded in a time compatible with those of the chip. Six months are expected to modify the different test boards, the firmware and software. The time estimated for the prototype test is in order of 3 months in laboratory.

The test bench based on the T2k one won't allow to study very carefully and deeply the asic performances. An other test bench must be build based on task 3.0 and task 4.0. A near collaboration is need. It will be the role of the project group to pilot efforts in this sense.

So responsible of the task will participate to the definition and the test of the ASAP board.

If the results are positives, the final validation will be made by testing the circuit with the detector in the GET environment.

In the case of unsuccessful, a second prototype phase will be launched.

Reliability of the design

The main important and critical part of the design concerns the SCA which will remain identical as the one in the AFTER circuit. It is clear that one discriminator per channel is a source of possible trouble and is not so trivial. But the risk can be minimized by using safety architecture, as differential structure for example and by taking some precautions in the layout of the chip. The laboratory has already designed this kind of functionality in several asics ([AGET2], [AGET3], [AGET4]) and has therefore a good experience in this domain.

Deliverables:

Detailed specifications. Test results of Submission. Documentation

- *Sub-task : Asic Support Board Conception*

Responsible: Jérôme Pibernat CENBG

The SE&A (Service d'Electronique et d'Automatisme) team of the CENBG/IN2P3 has an expertise in the design of frontend cards for high granularity nuclear detectors. The area of expertise covers the micro electronics analogue and digital. For the analogue part, the expertise is in the development of fast circuits with low noise. The digital expertise is related to highly integrated systems from high level languages (VERILOG, VHDL).

Main functions of the Front End Electronic card

The ASIC Support & Analog-Digital conversion (AsAd) card is connected on output of the detectors after passing through a protection circuit. Each AsAd hosts 4 AGET, each followed by an ADC 12 bits 25 MHz. The digital outputs of the 4 ADCs are transmitted by 8 differential lines with a maximum speed of 1.2 Gbit/s. In addition AsAd must manage and / or refer clock signals, multiplicity output, and slow control.

Apart from AGETs and ADCs, ASAD hosts:

- Auto test system for energy and time calibration
- Temperature gauge
- Power supply monitoring
- Board memory for identification
- Fully differential circuitry for transmission.

Task T-J01-3: Electronics and data acquisition

AsAd is very much akin to the FEC (front-end-card) of T2K with an equivalent geometrical layout. It is planned to develop a first version of AsAd for relatively low density of pads (1 pad/cm). A second version of AsAd will be also developed at a later stage for the 2p-TPC and ACTAR detectors which require high density inputs (5 pads/cm). In this case the card itself needs to be significantly smaller. In both cases cooling is necessary.

AsAd unique aspect

This frontal electronics is unique because for the first time around TPC detectors with various geometries and characteristics varied we have only one type of electronic which produces early digital signals. The combined functions will facilitate the setting of the experiments, the monitoring and the test. The high throughput capability allows efficient digital signal processing. We expect a cross talk lower than 0.1 % and a noise lower than 3000 e-.

Development planning

As noted above, the development of the cards AsAd requires a dense circuitry so that they can be used on high granularity TPCs. We therefore anticipate the development of 2 prototypes. The first will correspond to a moderate density of pads, while the second will concentrate on reaching the high density input requirements and a small format card. In 2009 we will simulate, design and built the first prototype. A bench test for the card will be designed and built in 2009 in parallel. It will be designed to allow production tests. The first prototype which will be furnished with AGET in mid 2009 will be tested before end 2009. Following positive tests of the first prototype, we will endeavour to reduce the format of the cards. We consider that the second prototype will be ready for testing in the laboratory at the end of 2010. Note: should the latter prove too difficult to achieve, at the design stage, an ASIC design of the external pre-amp + filter will be funded. This will be based on the pre-amp + filter of AGET itself. This option has to be studied as early as month 12.

Deliverables:

Specifications. First prototype tested. Contingency plan for ASIC PA. Second Prototype tested. Documentation.

iii. WBS 3.0 MULTIPLICITY, TRIGGER, TIME STAMPING AND EXTERNAL COUPLING ELECTRONICS

This work package is composed of two tasks, corresponding to functions as identified through the product breakdown structure. The ensemble will provide a complex trigger unit, capable of interfacing to other existing or foreseen systems.

This is the concretization of an effort of the whole French Nuclear community, by employing the latest FPGA technological know-how that has resourcefulness and flexibility well beyond the present GANIL Multiplicity Trigger. The unit in its form will be the base for a "universal" new system for GANIL. The other aspect is that the unit breaches a difficulty which GANIL and GSI have with respect to the Time-Stamping interfaces in developing the necessary hardware and firmware to allow integration of different systems.

- *Sub-task: Multiplicity, Trigger, Time stamping*

Responsible: Gilles Wittwer - GANIL

Objectives

Task T-J01-3: Electronics and data acquisition

The aim is to design and build the electronic device that, within GET, will manage the multiplicity, the conditions for the trigger, and the distribution of the clock on the whole system.

A particular attention to these aspects is due in a system destined to be coupled to the new-generation nuclear physics detectors. At 10000 channels or more, the traditional techniques of "Trigger" used in nuclear physics (analysis-windows + sequencer) are not sufficient any more today in terms of functionality and of integration.

The device is named "MUTANT" (MUltiplicity TrIgger ANd Time).

In more detail, the functions of MUTANT are:

- Regroup the numerical multiplicity at the highest level of the TPC;
- Choose the threshold of triggering and give the signal of "level 1" trigger;
- Distribute a clock to synchronise all the elements (CoBo AsAd, and AGET);
- Manage a system of "time-stamping" to give tags in every CoBo module essential in the tagging of the data, which will be sent to the acquisition computers. This allows, a posteriori, rebuilding the total event;
- Communicate with the external world via the module BEM (Back End Module) to ask and to accept a "super-decision" from the trigger of another detector and to receive the main clock (100/200 MHz).

Detailed work program

1. Design of the module

The specifications of the module will be defined based on the requirements of the different physics cases, as supplied through WBS 1.0.

The device will be an electronic standard NIM (Nuclear Instrument Module), using the most recent numerical techniques both at the hardware level and at the software package level. Its capacity will therefore be constructed according to following criteria:

- Use of the FPGA XILINX VIRTEX 4 or 5 with an integrated processor PowerPC;
- Linux operating system for the remote "slow control" of this card via an Ethernet link network with a standard protocol TCP/IP;
- Gigabit links with fibre optics to have communicate with the module BEM (to correspond to the need of galvanic insulation front-end/back-end while keeping high data flow over several tens of meters);
- Copper wires differential links in standards LVDS and LVPECL with CoBo modules.

The task responsible formulates a proposal for the design, which can be dynamically modified in the constant interaction with physics responsables under WBS 1.0. Technical compatibility and coherence with other modules is ensured by the Steering Committee.

The deliverables of this step are: a document with the technical specifications of the MUTANT module; a detailed estimate of the costs.

2. Realisation and tests of the prototype

The prototype is built using the technology already outlined above. A test bench is also built to validate the module.

A revision of the module could be necessary if some solutions do not perform as expected and specified. The work plan allows for contingencies (new prototype).

An expenditure report completes the deliverables.

• Sub-task : Back-End Module

Responsible Gilles Wittwer - GANIL

Objectives

The aim is to ensure an interface between the GET electronics, as coupled to a TPC detector, and other, ancillary equipment used in nuclear physics experiments (charged-particle and gamma-detector arrays, spectrometers). This will be achieved through the design and realisation of the BEM (Back-End Module).

The system in question will have the following functions:

- The possibility to be triggered externally;
- Synchronised clocks (internal or external);
- Coupling facilities to existing or new systems like CENTRUM, TDR, BUTIS;
- Provide the necessary links between MUTANT and other instrumentation;
- Allowing the tuning of the whole system (“inspection logic”).

Detailed work program

1. Design of the module

The specifications of the module will be defined based on the requirements of the different physics cases, as supplied through WBS 1.0.

The device will be an electronic standard NIM (Nuclear Instrument Module). The BEM has the following characteristics:

- Use of an FPGA Xilinx Virtex 4 or 5 with an integrated PowerPC;
- LINUX embarked operating system employed for the slow control via Ethernet with TCP/IP standards;
- Gigabit connection via optic fibre allowing a dialogue with MUTANT;
- Differential connection for the SMA for the clock entry-exit;
- Connectors and electrical standards that will allow it to be coupled with other systems (CENTRUM, TDR, BUTIS...).

Technical compatibility and coherence with other modules is ensured by the Steering Committee.

The deliverables of this step are: a document with the technical specifications of the BEM module; a detailed estimate of the costs.

2. Realisation and tests of the prototype

The prototype is built along with its test bench.

A revision of the module could be necessary if some solutions do not perform as expected and specified. The work plan allows for contingencies (new prototype).

An expenditure report completes the deliverables.

Unique Aspects of the combined MUTANT-BEM are:

We are building within the French Nuclear community a trigger unit employing the latest FPGA technological knowhow having resourcefulness and flexibility well beyond the present GANIL MULTIPLICITY TRIGGER. The unit in its form will be bases for developing a “universal” system for GANIL. The other aspect is that the units breaches a difficulty which GANIL and GSI have with respect to the Time-Stamping interfaces in developing the necessary hardware and firmware to allow integration of different systems.

Deliverables:

Simulations and written specifications. Evaluation of kit. Development of cards and testing of the MUTANT and BEM units in stand-alone and connected to CoBo . Beam tests with the unit. Documentation of the unit.

iv. WBS 4.0 DATA ACQUISITION HARDWARE**• Sub-task : The Concentration Board (CoBo).**

Responsible: Nathan Usher, MSU/NSCL

After the digitized signal leaves the front end ASAD board it will be processed in the concentration board (CoBo). The CoBo comprises an essential piece of the data taking chain because it is responsible for applying a time stamp, zero suppression and compression algorithms to the data. These operations will be conducted within an FPGA that is housed on the board. Due to the multiple times sampling features of TPC detectors large volumes of data are typically generated per event from the readout of each pad. However, a large fraction of these samples will not contain useable data. To reduce the volume of information that must be transmitted and stored a threshold will be applied to zero suppress empty bins. From simulations it is expected that this will result in a factor of 10-100 rejection ratio depending on the experimental applications. The ability to reconstruct zero suppressed data depends critically on the application of a uniform time stamp to all events. The clock time will be provided by the Mutant module to the CoBo. The FPGA chip selected to perform these tasks will be chosen to allow sufficient memory for applying an optional compression algorithm. This algorithm will apply a peak fitting routine to the data such that only the signal amplitude, width and centre of gravity are transmitted off of the CoBo. The advantage of such algorithms is that they result in an additional reduction in the volume of data transmitted. However, as such a reduction is not necessary for all experimental applications; this is considered to be an upgrade feature that is accommodated in the original design.

In addition to the data processing tasks performed by the FPGA, the CoBo will also serve as a communication intermediary between the AsAd and the outside world. The slow controls signals and commands to the AsAd will be transmitted via the CoBo. It is anticipated that these signals will include, but not be limited to, the clock signal, environmental monitoring, test pulse transmission, spy channels and power. Furthermore, the CoBo will handle the transmission of the trigger signal. Each AsAd will generate a digital pulse representative of the 3D channel occupancy. Because each CoBo card services 4 AsAds, within the FPGA of the CoBo these 4 signals will be summed before being transmitted onward to the Mutant for a trigger decision. The resultant trigger decision by the Mutant will be passed back to each AsAd via the CoBo. Should a positive trigger signal be received, the SCA stop write and read commands will be issued.

To accomplish the specified tasks, the CoBo card will be based around a Xilinx Virtex-5 FXT with embedded PowerPC processors and will also include flash memory, RAM buffer, clock buffer and the requisite signal and power connectors. The high performance FPGA contains high-speed programmable logic to perform zero suppression and time stamping on incoming data as it arrives. Following zero suppression, the PowerPC cores will run more advanced compression algorithms and prepare the data for transmission. Selection of the appropriate components is in progress. A Virtex-5 LXT development kit has been purchased to evaluate data throughput rates and aid in testing of potential board designs. It is anticipated that the data will be transmitted off of the CoBo via either gigabit Ethernet or gigabit optical fibre based on the requirements of the data acquisition systems of the individual laboratories.

Funds have been committed by the laboratory to cover the initial development costs of the CoBo. The CoBo development will be considered complete when the specified functionality has been incorporated and a data throughput rate of 1 kHz is achieved.

CoBo Unique Aspects:

The CoBo represents a unique advancement in electronics development in the intermediate energy Nuclear Science community because it provides digital signal processing at a data throughput rate of 1 kHz for a large data volume. Previous FPGA boards, such as

the T2K mezzanine module and the STAR readout card, have been internally limited to 10-100 Hz. A new generation of FPGA cards has just started to become available that allow event rates in the 1 kHz regime to be achieved. Two examples include the ALICE readout control units and the STAR DAQ1000 project. The CoBo is uniquely designed relative to these examples to meet the needs of the intermediate energy nuclear science community where reactions result in relatively low energy particles. These reaction conditions require the experimental capability of internal triggering since frequently the reaction products do not exit the primary detector. The CoBo represents the first FPGA card developed for a TPC that combines high data rates and internal triggering.

- *Sub-task : The Integration Board (InBo).*

Responsible G. Wittwer - GANIL

Objectives

The aim is to develop a device, through which the flow of data is received in a back-end PC for treatment. The device (Integration Board, InBo) will process the information collected from all the CoBos. Several levels of processing could be implemented, depending on the requirements for speed and data storage.

Detailed work program

1. Definition of the communication protocol

The InBo will typically be a commercial PCI-express card equipped with the last FPGA Xilinx Virtex 5 FXT. In order to ensure a very fast communication and at the same time galvanic insulation with the CoBos, the connection will be made through an optical link. The definition of the protocol for communication and data encapsulation is the first step of the InBo task. It has to take into account the requirements in terms of data compression and flow rate, and be compatible with the implementation on the CoBos. For this reason, the work will be carried out keeping a strong contact with the CoBo task.

The deliverable is a document describing the communication protocol (handshake, data encapsulation algorithm).

2. Definition of the data processing algorithms.

More than one optical link is usually present on an InBo card (most commonly, three links on the cards commercially available). Thus each card must be capable of collecting the information from the three links (i.e. three CoBos), verify synchronisation; make, if desired, a first low-level processing; and present the data to the PC CPU for further processing. In this architecture, more InBos are present on one computer. The amount of processing carried out at the InBo or at the PC level can thus be adjusted according to the needs (more fractioned for speed, concentrated at the highest level if only a selection of complex events is required). Possibilities for low-level data processing will be elaborated with the support from WBS 1.0 ("Physics validation") and eventually presented in a short report (deliverable).

3. Implementation of the protocols

This step is the effective firmware programming of the InBo. For its nature, it is possible to outsource the work to an external company – solutions from the manufacturers of the PCI-express cards have been explored and appear viable.

While the previous steps were based on general specifications of the PCI-express card that will constitute the InBo, for the present step a final choice needs to be made, since the programming is based on the possibilities offered by a specific card. It is thus at this stage that the PCI-express card for the prototype will be purchased.

The deliverable is the prototype InBo card with the software implemented.

4. Testing of the card

The card will be tested for its performances in relation with the defined protocols. A test bench will be set up at GANIL. The deliverable is the validation of the card.

v. WBS 5.0 DATA ACQUISITION SOFTWARE

• Sub-task : Test Bench Control and Command

Responsible: Frédéric Château CEA / DSM / IRFU / SEDI / LILAS

The LILAS (laboratoire Ingénierie Logicielle pour les Applications Scientifiques) of the CEA/DSM/IRFU/SEDI, and more precisely Frédéric Château and Shebli Anvar have developed two generic frameworks to address configuration and run control execution issues. Some of these software blocks are currently being used in the KM3 and T2K experiments, and some are scheduled to be. It could save a lot of time and development efforts to use them to handle the configuration and run control tasks for GET, especially for test benches development.

The goal

The goal is to base the run control and acquisition software of GET test benches, on these frameworks. F. Château will assist the software developers for the integration work. They will also provide support, like implementing new features to meet GET's needs, and fix bugs.

Description

The CCFG (Compound ConFiGuration) framework helps software developers, electronic engineers, and physicist to handle configuration in experimental physics projects. It simplifies and automates many tasks related to the management of configurations in such projects, and provides a powerful configuration semantics that makes it really fitted for distributed and complex systems in a scientific environment.

It is composed of several tools:

- A class library to read and write configurations in text files and in memory;
- A class library to use MySQL and Oracle databases to store and retrieve configurations;
- A Graphical User Interface program to enable end-users to display and edit configuration.

The DHSM (Data Host State Machine) framework helps software developers to quickly implement the state machine of the run control. It is an execution engine for state machines where the developer just has to setup the state machine: states, transitions, and so... then associate actions and data with them, and finally run it by sending events that will trigger transition crossing, state change and actions execution. All the execution logic and error handling is controlled by the framework.

One of the main features of the DHSM framework is the ability to run the state machine on a centralized distributed system. In such a system there is a master engine (typically the run control server) that controls an array of servant engines (typically acquisition nodes). All the hassle of doing network communications, state synchronization and distributed error handling is already managed by the framework (using ZeroC Ice and IceE middleware's).

All these tools run on Linux and Windows, and some parts of them run on VxWorks and RTEMS embedded systems.

Scheduled Work

The development of the run control server and acquisition software will rely on these frameworks. The run control server will use CCFG to read the configuration from the database or from files and send some parts of it to acquisition boards for their own initialization. The acquisition software will also use it to decode the configuration it receives and use it to initialize the hardware and the some software parameters. The run control user interface may also integrate CCFG widgets to enable the user to modify configuration on the fly before launching an acquisition. The aim is to implement very quickly small system to test the front end electronic (AGET + AsAd) and continue the development to reach the final software for many experiments.

The DHSM framework will be used both by the acquisition software and by the run control server. The first will use it to implement the acquisition state machine that consists of states like: On, Off, Idle, Initialized, Running, Paused, etc. The second will need it to define a similar state machine that will control the whole acquisition array.

- ***Sub-task Data acquisition software***

Responsible: Frédéric Saillant - GANIL

The objective of the task is to provide final data acquisition software, composed of tools, tested from the debugging of boards by hardware engineers. It is a key point that API's be used during the development phase and to build the final system. We will gain development time.

The data acquisition system should fit in the future "standard" GANIL data acquisition system and should use "standard" components of the GANIL system. The CCFG and DHSM frameworks could be used wherever the software design requirements and analysis will determine that their use will produce substantial gains in development efforts.

As the different boards of the system will be developed in different laboratories, the software delivered will have to be easily configurable to be adapted by the different teams.

The GET software DAQ system has basically three main functionalities:

Slow Control:

The Slow Control is in charge of setting up and monitoring the electronics: AGET ASICs, ASAD boards, COBO boards, INBO, MUTANT and BEM. The main functionalities Slow Control has to provide are:

- define which electronic boards are present in the system;
- initialize the different boards with correct values;
- save all the setup parameters of the whole electronics or a part of the electronics;
- restore a previously saved setup;
- monitor some key parameters of the boards (*e.g.* temperatures ...);
- handle error/ alarm events and pass them to the Run Control;
- accept some basic commands from the Run Control (setup, go, stop, get state).

The Slow Control system will be designed with a client/server approach. It will mainly consist in a Slow Control Core (SCC) communicating on one side with the different boards and on the other side with a graphical user interface which will behave as a client of the Slow Control Core. The communications between the Slow Control Core and its graphical interface could be implemented with the SOAP/XML network protocol and a WSDL (Web Service Description Language) interface.

The Slow Control Core could be based on the CCFG framework developed by the LILAS team to manage the configuration of the electronics.

Having in mind to put as much intelligence as possible inside the electronics, boards containing a Xilinx Virtex FPGA with a PowerPC core could embed a network command server running under the Linux operating system, which provides advanced network services (TCP/IP, HTTP, SOAP...). GANIL team is going to test very soon the ENX command server designed for the AGATA project. This server should be available at the beginning of 2009. We therefore propose that all the electronics boards embed the same ENX server.

Run Control:

The Run Control has the main purpose to control and monitor the DAQ components. It coordinates the several activities necessary to put the GET system and its data acquisition software into operational state. Actions like initialization, setup, start and stop of the data acquisition are performed by the operator through the Run Control system. It interacts with the Slow Control system in order to assure the correct configuration and setup of the electronic devices, before data taking is started. It also provides the monitoring of the acquisition, error report and logging capabilities.

The main tasks are outlined here:

- configure the DAQ for a run by selecting data flow active components;
- save/restore a configuration;
- basic commands to control all the active components (setup, start, stop);
- monitor the DAQ (status, data rates);
- handle error/info messages;
- log book;
- display spectra.

As the Slow Control, the Run Control system will be designed with a client/server approach. It will also consist in a Run Control Core (RCC) communicating on one side with the data flow active components and on the other side with a client graphical user interface. The communications between RCC and its graphical interface could be implemented with the SOAP/XML protocol and WSDL interface.

The RCC could be based on the general purpose RCC skeleton currently developed at GANIL. CCFG and DHSM LILAS frameworks could also be integrated in this development.

Data Flow:

The goal is to process the data flow which is coming from the detectors up to the data storage. Data sources are the detectors after their front-end electronics (AsAd boards). The AsAd outputs are collected by the COBO boards. Then all data coming out of the COBO boards are merged together thanks to an Event Builder taking into account the physics correlations provided by the MUTANT board. At the end of the chain, data have to be provided to the physicists in an understandable and user-friendly way thanks to a Data Format library, and are stored on a large disk array.

The data flow will be based on the NARVAL data acquisition system currently used at GANIL. It is distributed and entirely configurable software which can be easily adapted to the different configurations. Some specific actors will have to be designed to answer to the different steps of the project, especially for the event builder of the whole system.

Work plan

The main steps of the work are listed below:

- Embedded Linux + command server for Virtex.
- Specific embedded drivers for each board (ASAD, CoBo, InBo, MUTANT, BEM).
- SCC specific + GUI (ASAD, CoBo, InBo, MUTANT, BEM).
- RCC specific.
- Event Builder (GET).

Task T-J01-3: Electronics and data acquisition

- Calibration.

This list considers that developments are based on standard GANIL + LILAS tools.

Finally, the data acquisition system of GET has to include a set of tools needed for doing the first online analyses of the tracks associated with the energy losses of ions of interest into the TPC. This information is crucial for the tuning of the detection setup and the checking of the data.

The first tools are the calibration procedures for the measure of the linear response function of the electronic chain and its non-linearity and for the control of its stability with respect to the experimental conditions of the data runs. The large number of channels and the scalable-design of the electronics imply the developments of specific software and hardware and the development of physical based innovative automatic procedures. These elements will also provide to the physicists the synthetic overviews of the system, the error diagnostics and warnings. Some of them are needed at different stages of the R&D especially for bench tests.

Finally, a large amount of the data flow includes trivial events, the beam passing into the TPC. The set of interesting events could represent a tiny part of the recorded events. In case of high counting rates, especially in a standalone mode without external trigger, a software selection should be needed for reducing the data flow or useful for tagging the events. This selection will provide events for the data analysis and allow a fast data readout as well. Different selection methods can be investigated (binary collision, angular correlation) in complement of the trigger selection (multiplicity, triggering pattern) leading to common developments of fast and accurate algorithms.

The DAQ system as presented in its different components (slow control, run control and data flow) has the adaptability and the performance for adding the functions of calibration and event selection. These functions are needed by the data analysis which is driven by the physicists requiring competences and specific developments of the data acquisition of GET.

vi. WBS 6.0 QUALITY AND DOCUMENTATION MANAGEMENT

Responsible: Frédéric Druillolle -CEA/DSM/IRFU/SEDI/LDEF

Objectives:

This is a collaborative project between IRFU, CENBG, MSU and GANIL. It will involve comparable, parallel efforts from four institutions. The efforts on the project are divided between institutions in a way that matches well to the expertise of the personnel and that allows efforts to proceed in a parallel manner without great interdependence. Never-the-less, close collaboration and effective communication are essential to coordinate efforts and keep the project on schedule. We will communicate by frequent phone and video conferences, emails, and regular visits between institutions. We also utilize web-based tools, such as WiKi and EDMS that keeps a cohesive record of all developments for all members of the collaboration to follow.

Detailed work program:

Each responsible of task has to provide a number of document to the project group. The list of document is listed below:

- STB: Spécification technique des besoins (Requirement):
- CDR : Conceptual Design Report :
- IDR: Interface definition Report:
- TDR : Technical Design Report :
- TR: Test Report:
- PRR: Production Readiness Report:

Task T-J01-3: Electronics and data acquisition

The framing, versioning and storage of the documentation will be created by the WBS 6.0 task members in agreement with each task leaders. The aim is to have a steady documentation to check the coherence between interfaces, to detect defaults and incoherence between products.

A second goal is the organization of review to prepare the prototype manufacturing. At least two reviews are mandatory. One concerns the description of each product before realization. The second is the production readiness review for the prototype of the system.

One important task will be the review and the validation of each paper proposed to be published like a publication committee has to do.

The last task is to maintain web-based tools for keeping aware the collaboration about each part, about the consistent schedule, stakes and due dates during the project.

vii. WORK PACKAGES SUMMARY

<u>Task id</u>	<u>Product Name</u>	<u>Description</u>	<u>Responsible</u>
WBS_0.0	Steering Committee (Management)	Pilots each task and controls the interface between products.	E. Pollacco (IRFU) JL Pedroza (CENBG)
WBS_1.0	Physics Validation	To check the appropriateness of the GET specifications and physics requirements for three existing TPCs (AT-TPC, MAYA, CENBG-TPC).	R. Raabe (GANIL)
WBS_2.0	Front End Electronic	Builds the ASIC and the near asic environment and Build the ASIC support card with all necessary added functions (protection, trigger and ADC, slow control)	J. Pibernat (CENBG)
WBS_3.0	Multiplicity, time and trigger conception	Builds the system of time and trigger management and manages the interface with other products of the system	G. Wittwer (GANIL)
WBS_4.0	Data Acquisition Hardware	Builds the cards which handle the data flow	N. Usher (MSU)
WBS_5.0	Data Acquisition Software	Develops all the Applied Programmable Interface necessary to build test bench and final acquisition software.	F. Saillant (GANIL)
WBS_6.0	Quality and documentation management	Organizes the review, to follow the document of each work package, takes care of the storage of the documentation and the quality process of the project.	F. Druillole (IRFU)

2 PLANNING OF TASKS, DELIVERABLES AND MILESTONES

2.1 TASKS AND THEIR INTER-RELATIONSHIP

To reach the required deliverables the project is divided into 10 sub-tasks which are grouped under 6 basic Work Packages (Section 3.3). The division is done by unit module (described

above). The inter-relation between of the tasks can be understood through the functions required (fig. 3.1) and in table giving the calendar (above). The efforts on the project are divided amongst institutions in a way that matches well to the expertise of the personnel and the laboratory as a whole. It allows each partner involved comparable, parallel and necessary efforts. Further, it leaves a challenge for each partner to achieve. The studied choice of division and allotment allows efforts to proceed in a parallel manner without great interdependence.

viii. TASK SEQUENCING

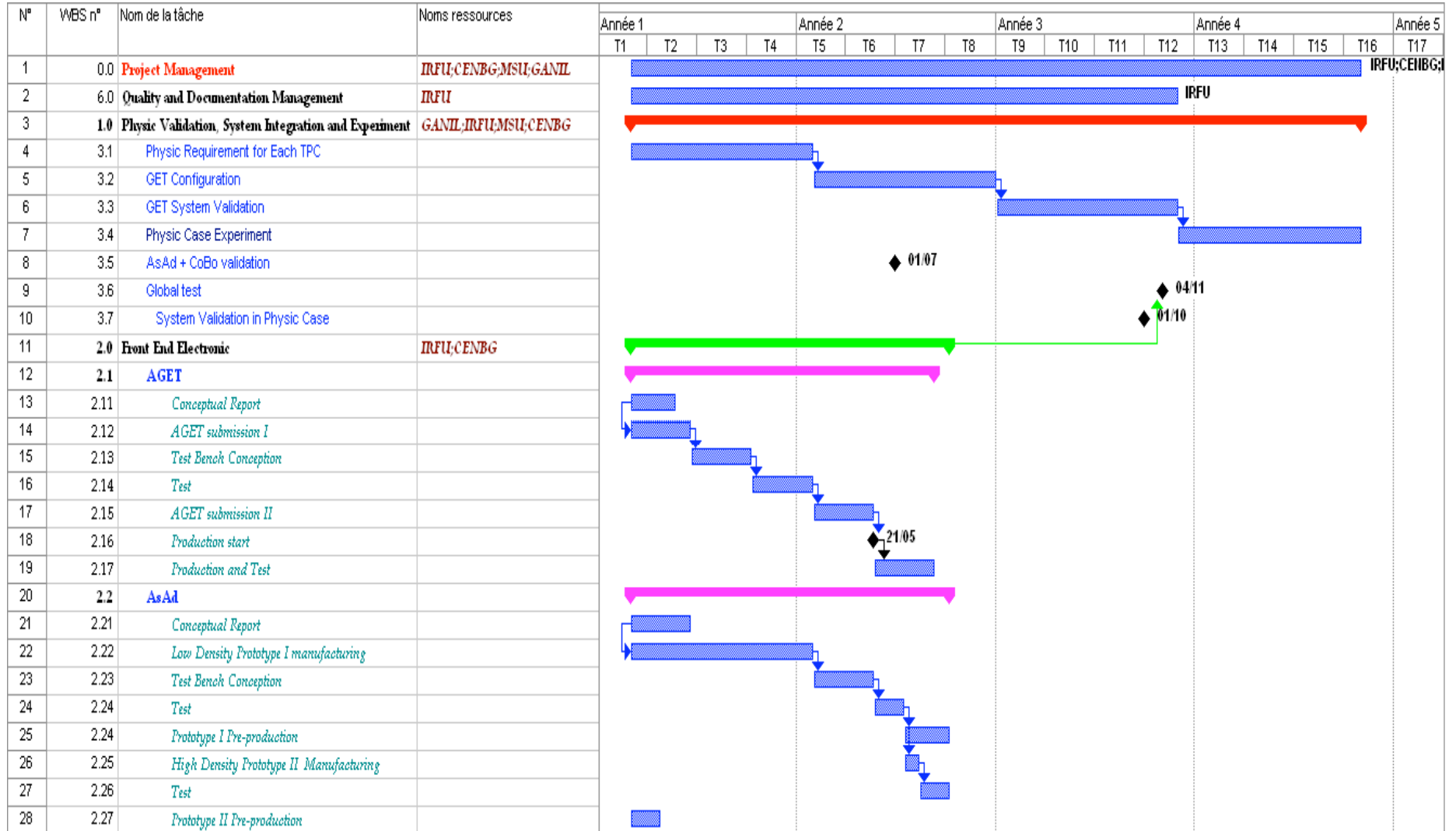
The Task Sequencing is eased by the fact that each principle unit (AsAd, CoBo ...) has a test bench development. However, the conception of the CoBo board (PBS_2.0) depends on the implementation of the ASIC support card (PBS_1.2) because of the ADC controller. This front end card, AsAd, is constrained by the trigger policy and the geometry of the readout detector plan (number of pixels, size) and should be done only when the AGET asic is ready to be built (PBS_1.1). MUTANT/BEM boards (PBS_4.1 and 4.2) are reasonably independent to build because they constraint the trigger implementation in other board such as the front end and back end boards.

The firmware for the testing of the prototypes is non-critical in the sense that most of it is almost available for the initial tests of AGET. The software development for the data merging etc., is rather independent until hardware exists. At this time, real implementation must be done to test each board and the final system.

ix. RISK ASSESSMENT

The risks are in general relatively small because each of the founding elements being attempted have been, by and large achieved in previous studies, for example in HIRA, MUST2, T2K and other projects. However what is particularly innovative is the combined concepts and consequently a risk is the large numbers involved, the level of control per channel as well as the speed of the data transfer and the multi-level trigger. A concern is the selective-readout however IRFU has build an asic with such a facility. Another aspect which requires vigilance is that the tasks/work packages are interdependent particularly in the final stage, thus possibly leading to costly delays. Counter actions are taken to require, when as possible, bench testing as well as to introduce simple procedures that will allow a large fraction of the system to function without certain elements. Finally, but of primordial importance, the insistence of having regular meeting to keep the whole group at breast with the progress made.

Task T-J01-3: Electronics and data acquisition



Task T-J01-3: Electronics and data acquisition

N°	WBS n°	Nom de la tâche	Noms ressources	Année 1				Année 2				Année 3				Année 4				Année 5
				T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	T17
29	3.0	Multiplicity, Trigger Management	GANIL,MSU																	
30	3.1	MUTANT																		
31	3.11	Conceptual Report																		
32	3.12	MUTANT prototype manufacturing																		
33	3.13	Test Bench Conception																		
34	3.14	Test																		
35	3.15	Prototype II Pre-production																		
36	3.16	Production start																		
37	3.17	Production and Test																		
38	3.2	BEM																		
39	3.21	Conceptual Report																		
40	3.22	BEM prototype manufacturing																		
41	3.23	Test Bench Conception																		
42	3.24	Test																		
43	3.25	Production start																		
44	3.26	Production and Test																		
45	4.0	Data Acquisition Hardware	GANIL,MSU																	
46	4.1	CoBo																		
47	4.11	Conceptual Report																		
48	4.12	CoBo prototype manufacturing																		
49	4.13	Test Bench Conception																		
50	4.14	Test																		
51	4.15	Production start																		
52	4.16	Production and Test																		
53	4.2	InBo																		
54	4.2.1	Conceptual Report																		
55	4.2.2	CoBo prototype manufacturing																		
56	4.2.3	Test Bench Conception																		
57	4.2.4	Test + Bug Correction																		
58	4.2.5	CoBo prototype II manufacturing																		
59	4.2.6	Test																		
60	4.2.7	Production start																		
61	4.2.8	Production and Test																		
62	5.0	Data Acquisition Software	IRFU,GANIL																	
63	5.1	Test Bench Software																		
64	5.2	Experiment Control & System Security																		

List of acronyms

AGET	ASIC for GET
ACTAR:	Active Target
ASAD	Asic Support Analog Digital
ASIC:	Applied Specific Integrated Circuits
AT-TPC:	Active Target-Time Projection Chamber
2-p TPC:	Two proton Time Projection Chamber
BEM:	Back End Module
BTDS:	Beam tracking detectors
CoBo:	Concentration Board
COTS:	On the market available units.
CENTRUM, TDR, BuTiS:	Time stamping units in differenet labs.
GET	General Electronics for TPCs
GLAD:	Large Acceptance Dipole
InBo:	Integration Board
MUST2:	Murs a Strips 2, (2: telescope of second generation)
MUTANT:	MUtiplicity Trigger ANd Time
RIBF:	Radioactive Ion Beam Facility
TPC:	Time Projection Chamber
VAMOS:	Variable Mode Spectrometer (GANIL)