

# First Steps towards FAIR Controls

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## 1. Introduction

In 2004 the work on FAIR controls has started. Among the core requirements is parallel handling of different beams, so that FAIR accelerators will be able to serve up to 4 experiments independently. To this end, the system architecture is crucial as well as the design of the timing system. Moreover, effective set-up procedures and surveillance mechanisms are needed to operate the accelerators with a small operator crew.

## 2. Design Concepts

The system will be designed as a decentralized distributed system. A sketch of the architecture of the control system is shown in Figure 1, specifying the structure of three layers of applications, device presentation and equipment control.

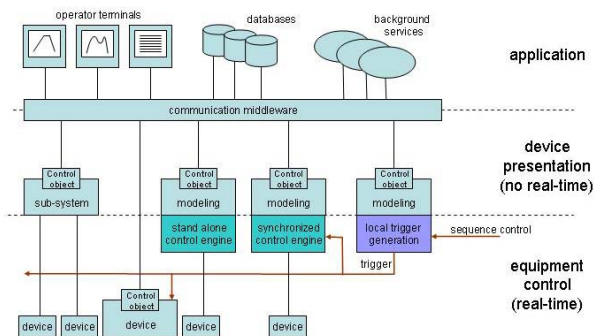


Figure 1: Architecture of the Control System

The timing system foresees a central sequencing unit for the coordination of the local timing generators. Information about the next beam to be handled and timing events for the actual accelerator cycle will be distributed by the local timing generators; see also Figure 2, where the interplay in this hierarchical timing structure is illustrated.

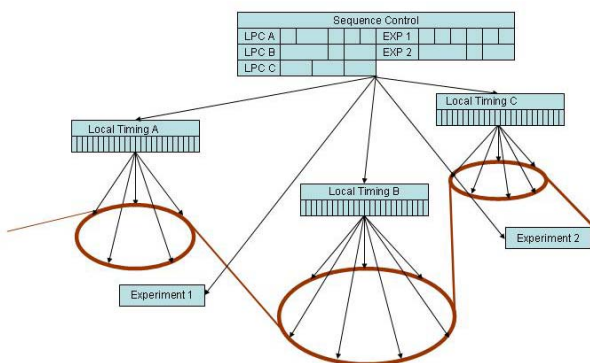


Figure 2: Hierarchical Timing Structure

The development of the system core and front-end side will be twofold: On the one hand an evaluation of recent

technologies is in progress, including control systems, e.g. ACS, and also timing components or interfacing technology. First steps in the evaluation of embedded processors have been done and will be followed up by FireWire technologies. Since, on the other hand the requirements for FAIR controls are being gathered; a combination of both sides will lead to the development of a general layout of the system in a modern way.

Operating FAIR will require efficient operation tools to support set-up and optimization of set-values for the equipment. Services will be provided to help both operators and equipment specialists in understanding the many complex situations which will arise during commissioning or operation of the FAIR accelerators.

## 3. SIS18 Upgrade

Since SIS18 will serve as injector for FAIR, its upgrade to higher repetition rates and intensities is crucial [1]. In order to increase the SIS18 repetition rate via 1 Hz up to 4 Hz, not only the ramp rate must be increased, but also the logistics of the SIS cycle must be overhauled with the goal to overlap the different phases: e.g. extraction must be prepared during the acceleration phase.

Furthermore, a number of machine experiments and technical studies have been performed to study and improve the behavior of the synchrotron during faster ramping. While the technical equipment is capable of running the full design ramp rate of 10 T/s, the beam cannot be accelerated so far.

## 4. Summary and Outlook

Preliminary concepts for the FAIR control system have been developed[2]. Due to the complexity of the system, it is crucial to discover potential weak points as soon as possible, in particular by checking critical parts in a running environment. Since the present GSI facility is in many aspects similar to FAIR, it provides an outstanding test environment.

An early completion of consolidation of the control system will help to free resources for the FAIR project. As emphasized above, it will also serve as a 'real-life' test bench of controls to analyze the present status of GSI accelerators and to shed more light on necessary measures to fulfill the various requirements for an efficient operation of the FAIR facility.

## References

- [1] P. Schütt, R. Bär, B. Franczak, U. Krause, A. Redelbach, S. Richter, V.R.W. Schaa, W. Schiebel: "Schneller Pulsbetrieb am SIS", GSI internal Report, 2004.
- [2] P. Schütt, U. Krause, W. Schiebel, R. Bär, B. Franczak, L. Hechler, A. Redelbach, S. Richter, V.R.W. Schaa: "Technical Report on Controls, Commissioning and Operation of the Accelerators of FAIR", GSI, 2005.